CS 254
DIGITAL LOGIC DESIGN

Universal Asynchronous Receiver/Transmitter

Team Members

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Goal

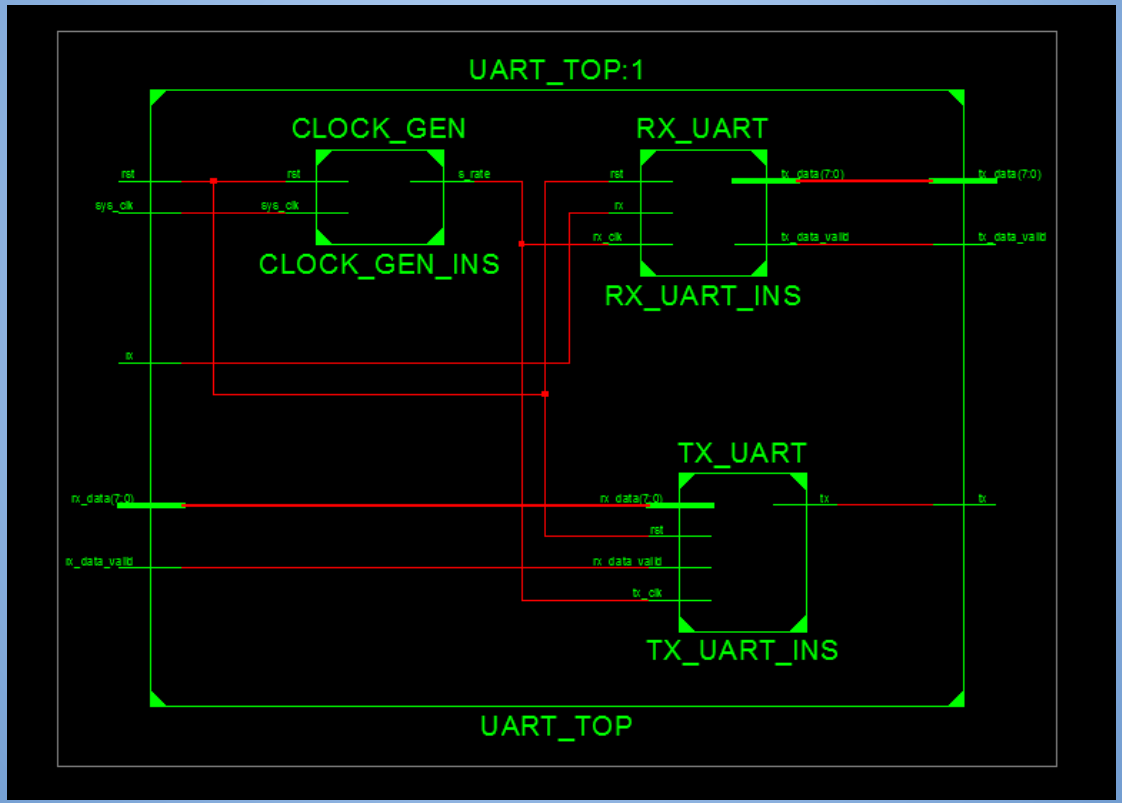
To design and simulate universal asynchronous receiver/transmitter circuit (UART) in Xilinx ISE and Implement the simulated design on ATLYS board.

RTL Components

The UART Circuit consists of 3 register level modules:

1. Clock Generator
2. Transmitter
3. Receiver

RTL schematic without Connecting TX_DATA to RX_DATA



Clock Generator

Inputs:

1. reset (rst)
2. clock (sys_clk)

Output:

1. s_rate

The clock generator module takes system clock as input and convert this rate to sampling rate.

Baud rate = 19200 Hz (1)

*Sampling rate = 16 * Baud rate (2)*

clock freq = 100 MHz (3)

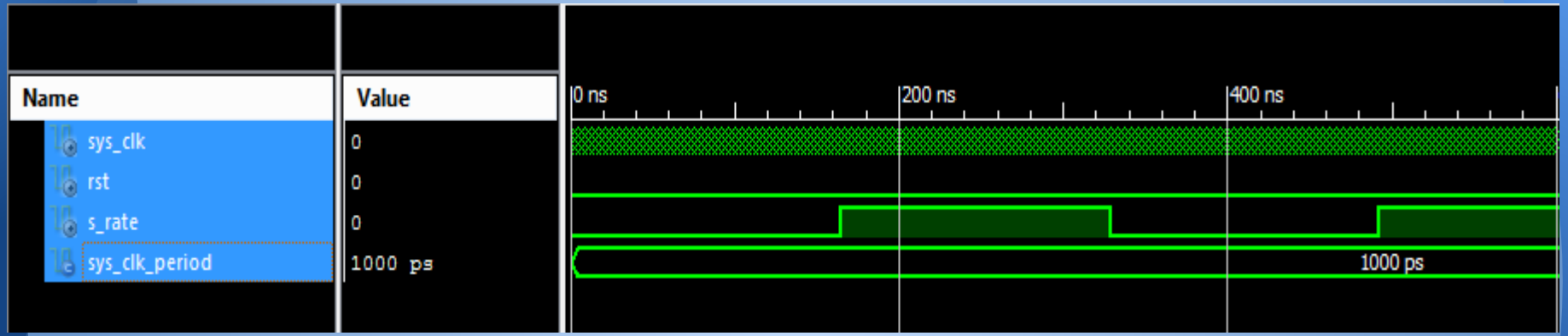
Using the above equations we can calculate that in approximately 326 clock cycles of system clock sampling should be done once.

So we keep a counter of 8 bit. When the counter reaches 163(0b10100011) we need to change output clock signal.

In this way we can we can generate a more slower clock with our faster system clock.

‘reset’ signal asynchronously resets s_rate to zero.

Simulation of Clock generator



sys_clock Time Period = 1 ns

*1/s_rate = 1 ns * 326 = 326 ns*

Transmitter

Inputs:

1. reset (rst)
2. rx_data_valid
3. rx_data(7:0)
4. tx_clk

Output:

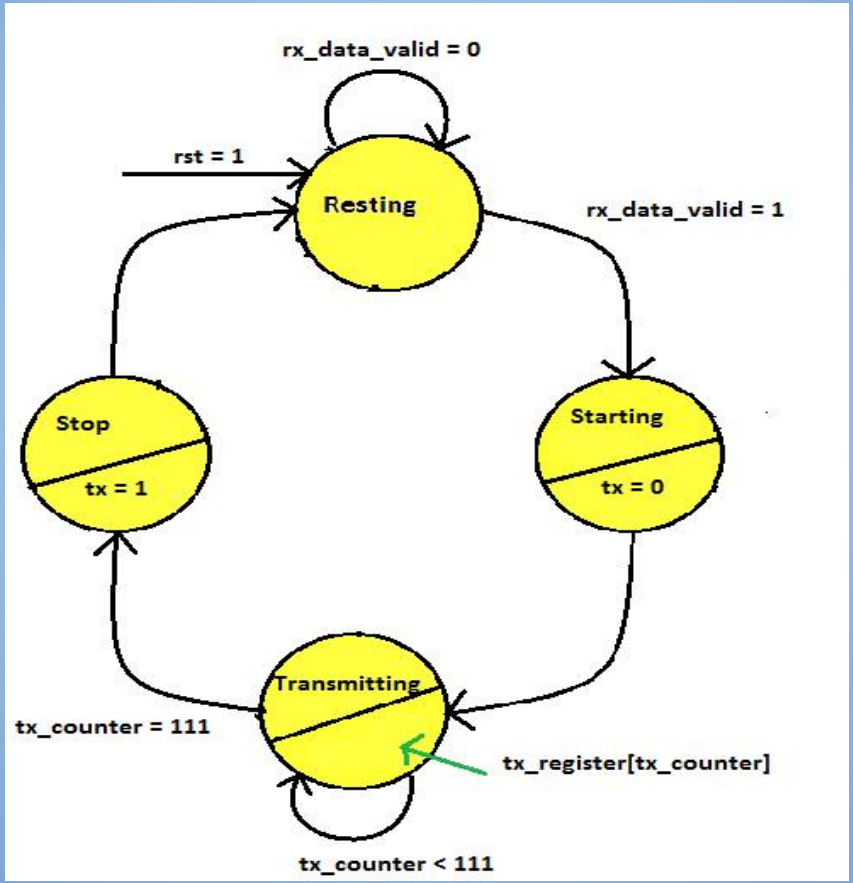
1. tx

Data is transmitted in serial fashion. Transmitter will get 8-bit data(rx_data) in parallel which should be transmitted 1-bit as(tx) over 1 /baud rate time or over 16 times sampling cycle. The transmission character is composed of an 8-bit data byte, sent LSB first, proceeded by a start bit (LOW) and followed by a stop bit (HIGH).

Transmitter consists of 4 states:

1. Resting- Idle state, tx is 1, goes to ‘starting’ state when rx_data_valid is 1 for 1/ Baud rate time.
2. Starting- tx is set to zero for 1/baud rate time, then moved to ‘transmitting’ state.
3. Transmitting- tx is set to rx_data[i] (i = 0 to 7) each for 1/Baud rate time, then it goes to ‘stop’ state.
4. Stopping- tx is 1 for 1/baud rate time then goes to ‘resting’ state.

State Diagram for Transmitter

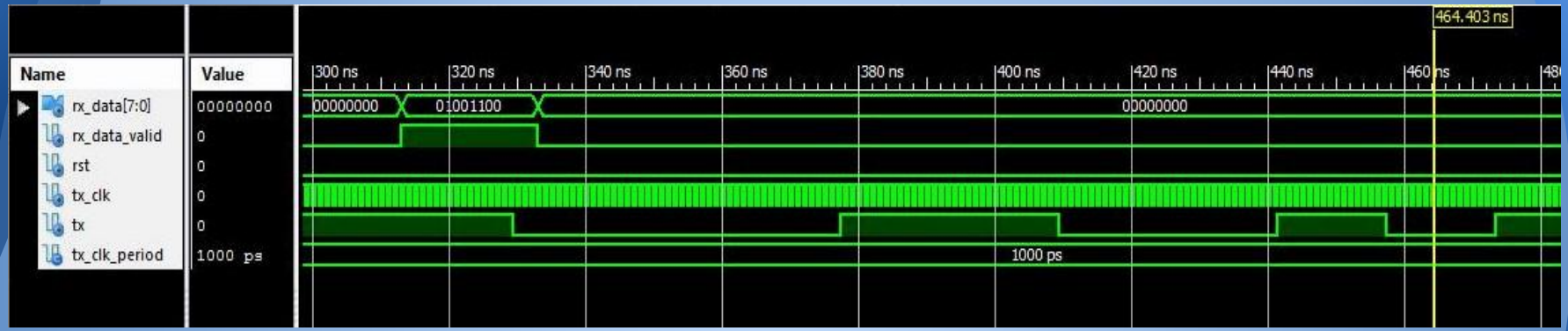


Implementation

Two counters are kept:
1. For keeping the sampling of a bit [3:0] (0 to 15).
2. For keeping the number of bits transmitted [2:0](0 to 7).

Reset signal asynchronously resets the circuit.

Simulation for Transmitter Module



Receiver

Inputs:

1. reset(rst)
2. rx
3. rx_clk

Outputs:

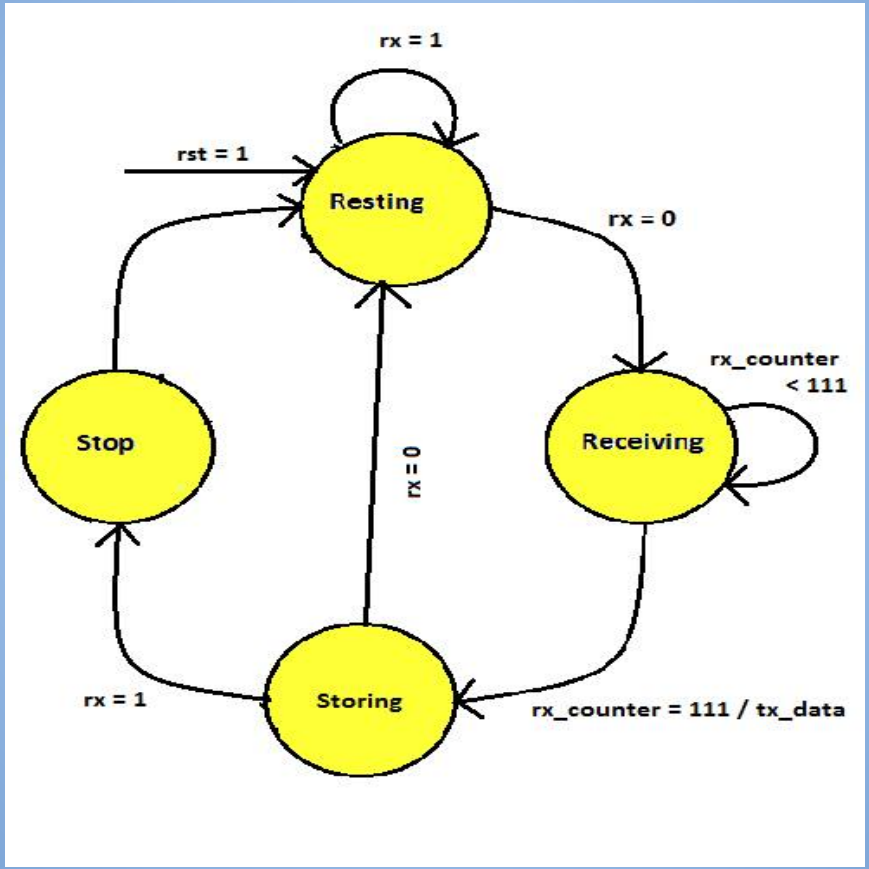
1. tx_data[7:0]
2. tx_data_valid

Data is received in serial fashion. Receiver will receive 8-bit data serially(rx) which should be given as 1-byte (tx_data) in 1/ Baud rate cycle or over 16 times sampling cycle. When no character is being transmitted, the line remains idle (HIGH).

Receiver consists of 4 states:

1. Resting- Idle state, tx_data_valid is 0, goes to ‘receiving’ state when rx is 0 for 1 Baud cycle.
2. Receiving- As rx comes tx_data[i] is set to rx value each one of the 1/Baud rate time, after 8 cycles then it goes to ‘storing’ state.
3. Storing- tx_data_valid is set to 1 for 1/Baud rate time. Then it goes to stop state.
4. Stop- waits for 1/Baud rate time then goes to ‘resting’ state.

State Diagram for Receiver

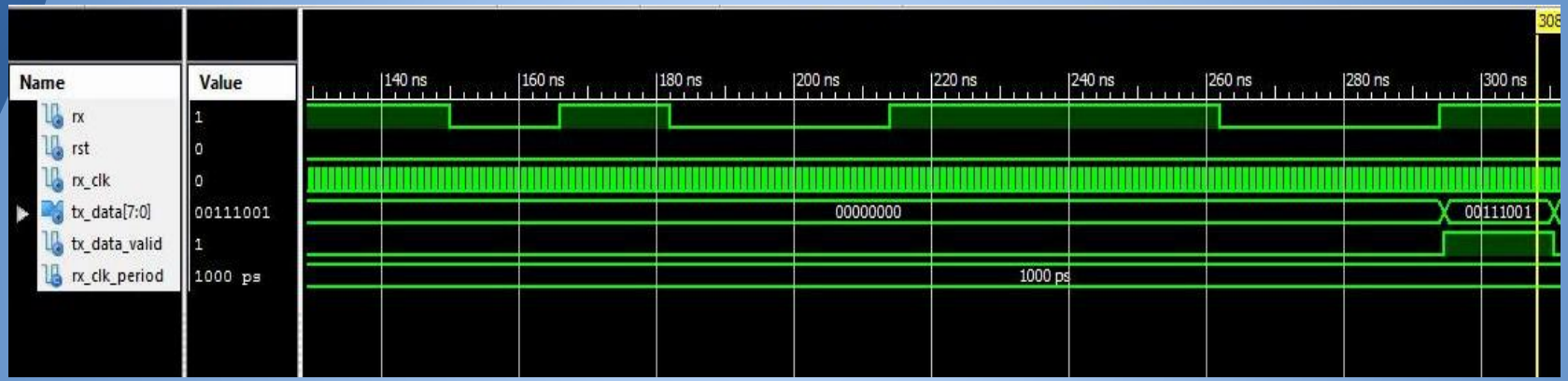


Implementation

Two counters are kept:
1. For keeping the sampling of a bit [3:0] (0 to 15). The 8th bit of this sample is taken as rx
2. For keeping the number of bits received [2: 0](0 to 7).

Reset signal asynchronously resets the circuit.

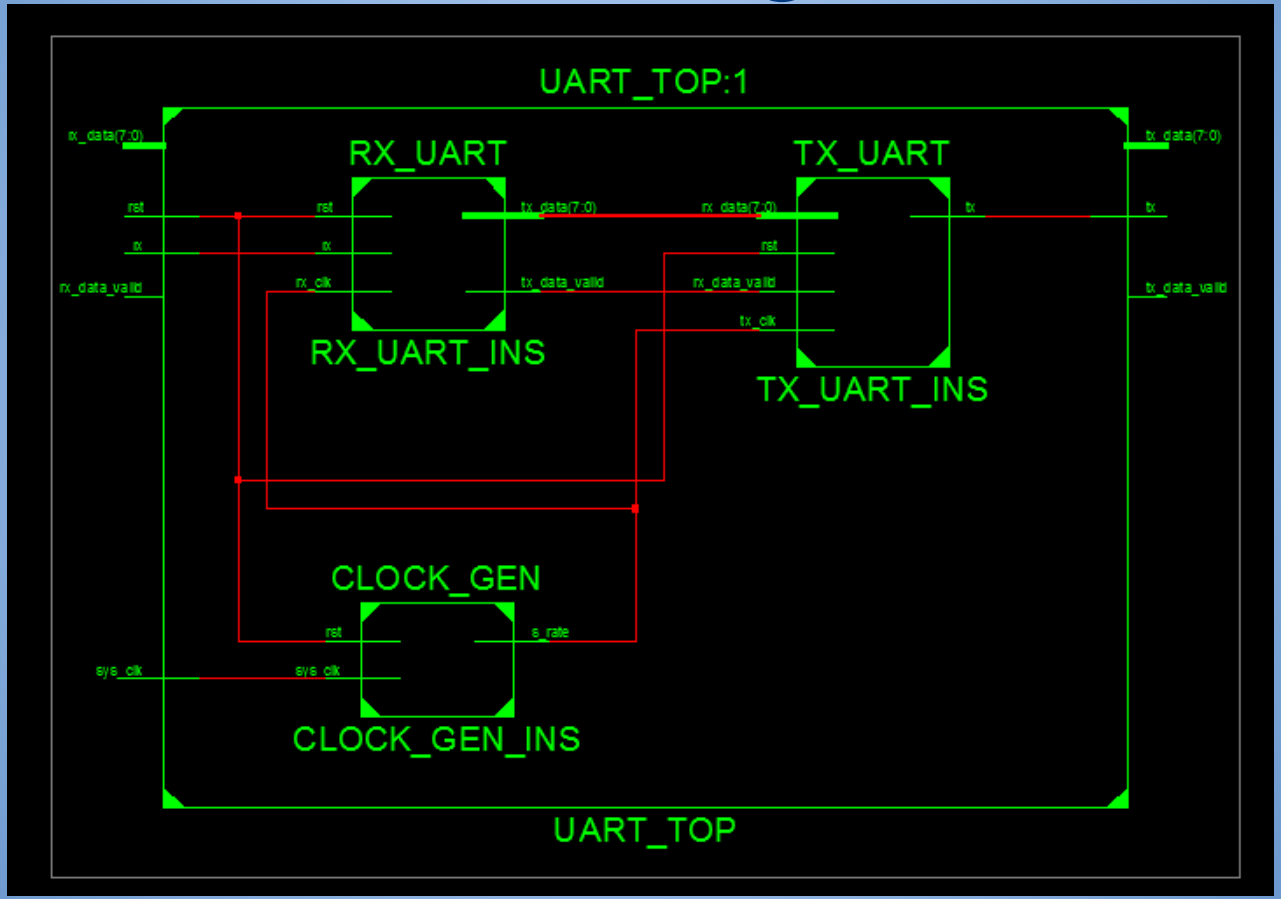
Simulation for Receiver Module



Testing on Board

While testing on board, the output of receiver is send to transmitter.
i.e TX_DATA is connected to RX_DATA and TX_DATA_VALID to RX_DATA_VALID for loopback purposes.

RTL while testing on board



In this case, TX_DATA and TX_DATA_VALID has no use as the outputs of receiver are connected directly to inputs of transmitter.

Connecting this to teraterm with input/output UART ports in UCF files will give the correct result.

Contributions

1. 130050001- Ghurye Sourabh Sunil
TX module, TX module testbench, UART top module, report
2. 130050023- Nikhil Vyas
RX module, RX module testbench, clock generator, UART top module TB
3. 130050037- Utkarsh Mall
TX module, RX module, clock generator TB, presentation
4. 130050038- Mayank Sahu
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