Side-channels

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Recall from last time:

Pick target(s) → Choose launch parameters for malicious VMs → Each VM checks for co-residence → Frequently achieve advantageous placement

This shouldn’t matter if VMM provides good isolation!
Today

• Flush+Reload
  – Covert channel
  – As a side-channel

• Meltdown
The RSA trapdoor permutation

\[ \text{pk} = (N,e) \quad \text{sk} = (N,d) \quad \text{with} \quad ed \mod \phi(N) = 1 \]

\[ f_{N,e}(x) = x^e \mod N \quad g_{N,d}(y) = y^d \mod N \]
Textbook exponentiation

How do we compute $h^x \mod N$ for any $h \in \mathbb{Z}_N^*$?

**Exp(h,x,N)**

$X' = h$

For $i = 2$ to $x$ do

$X' = X' \cdot h \mod N$

Return $X'$

Requires time $O(|\mathbb{Z}_N^*|)$ in worst case.

**SqrAndMulExp(h,x,N)**

$b_k,\ldots,b_0 = x$

$f = 1$

For $i = k$ down to 0 do

$f = f^2 \mod N$

If $b_i = 1$ then

$f = f \cdot h \mod N$

Return $f$

Requires time $O(k)$ multiplies and squares in worst case.
SqrAndMulExp(h,x,N)

\[ b_k, \ldots, b_0 = x \]
\[ f = 1 \]

For \( i = k \) down to 0 do

\[ f = f^2 \mod N \]

If \( b_i = 1 \) then

\[ f = f \cdot h \mod N \]

Return \( f \)

\[ f^3 = 1 \]
\[ f^2 = h^2 \]
\[ f^1 = (h^2)^2 \cdot h \]
\[ f^0 = (h^4 \cdot h)^2 \cdot h = h^8 \cdot h^2 \cdot h \]

\[ x = \sum_{b_i \neq 0} 2^i \]

\[ h^x = h \sum_{b_i \neq 0} 2^i = \prod_{b_i \neq 0} h^{2^i} \]

\[ h^{11} = h^{8+2+1} = h^8 \cdot h^2 \cdot h \]

\[ b_3 = 1 \quad f_3 = 1 \cdot h \]
\[ b_2 = 0 \quad f_2 = h^2 \]
\[ b_1 = 1 \quad f_1 = (h^2)^2 \cdot h \]
\[ b_1 = 1 \quad f_0 = (h^4 \cdot h)^2 \cdot h = h^8 \cdot h^2 \cdot h \]
SqrAndMulExp(h,x,N)
\[ b_k, \ldots, b_0 = x \]
f = 1
For i = k down to 0 do
  f = f^2 \mod N
  If b_i = 1 then
    f = f*h \mod N
Return f

\[ x = \sum_{b_i \neq 0} 2^i \]

\[ h^x = h \sum_{b_i \neq 0} 2^i = \prod_{b_i \neq 0} h^{2^i} \]

What side-channels might arise?
• Timing
• CPU state (caches, branch predictors,...)
• Power
Attack setting

Co-located placement on cloud instance

- RSA-Decrypt takes adversarially supplied ciphertext $c \in \mathbb{Z}_N^*$ and computes $c^d \mod N$

- Attacker running on same server, in different VM (or process)

Where would this come up in practice?
(Part of) TLS handshake for RSA transport

Client

Pick random Nc
Check CERT using CA public verification key
Pick random PMS
C <- E(pk,PMS)

Server

ClientHello, MaxVer, Nc, Ciphers/CompMethods

ServerHello, Ver, Ns, SessionID, Cipher/CompMethod
CERT = (pk of bank, signature over it)

C

PMS <- D(sk,C)
Cache-based side channel attacks

• A long literature on cache side channel attacks
  – Percivel 2005: RSA side channels
  – Tromer et al. 2005: AES side channels
• Today: particularly simple one by Yarom and Faulkner useful in PaaS clouds

```
SqrAndMulExp(h,x,N)

b_k,..,b_0 = x
f = 1
For i = k down to 0 do
  f = f^2 mod N
  If b_i = 1 then
    f = f*h mod N
Return f
```
Towards Prime+Probe

Suppose victim and attacker shares a core

Also sharing L1 instruction & data caches
Prime+Probe protocol

- Attacker VM
- Victim VM

L1 instr cache (each row represents cache set)

- Fast
- Slow

Main memory

- Timings correlated to (distinct) cache usage patterns of S, M operations
- Can spy frequently (every ~16 μs) by exploiting scheduling
Prime+Probe limitations

• Originally worked only for L1 caches
  – Some recent work extending to LLC in certain settings
  – Multi-core settings difficult but feasible in lab (Zhang et al. 2012)

• Lots of noise from various sources

• State-of-the-art:
  – Sinan Inci et al. 2016 “Cache Attacks Enable Bulk Key Recovery on the Cloud”
Towards Flush+Reload

Deduplication-based memory page sharing (Linux, KVM, VMWare)

- Duplicate memory pages detected, physical pages coalesced
- Virtual address spaces different, but mapped to same physical addresses

Inclusive cache architecture
Towards Flush+Reload

Deduplication-based memory page sharing (Linux, KVM, VMWare)

- Duplicate memory pages detected, physical pages coalesced
- Virtual address spaces different, but mapped to same physical addresses

Inclusive cache architecture
Flush+Reload protocol

- Flush from LLC memory line of interest
- Wait
- Time reloading memory line

Not-accessed by victim

Accessed by victim
Flush+Reload protocol

- Attacker VM
- Victim VM
- Main memory
- S instr
- M instr
- Fast
- Slow

- Runs (S) operation
- Interrupt
- Scheduling order on CPU core

- Fast time on S instr means S op

L1 instr cache (each row represents cache set)
Flush+Reload protocol

- Runs (S) operation
  - Attacker VM
  - Victim VM
- Interrupt
- Runs (M) operation
  - Attacker VM
  - Victim VM
  - Scheduling order on CPU core

- Fast time on S instr means S op
- Fast time on M instr means M op
Attacking Square and Multiply

\[
\text{SqrAndMulExp}(h, x, N)
\]

\[
b_k, \ldots, b_0 = x
\]

\[
f = 1
\]

For \(i = k\) down to 0 do

\[
f = f^2 \mod N
\]

If \(b_i = 1\) then

\[
f = f * h \mod N
\]

Return \(f\)
Flush+Reload applicability

- Immediately used in a large number of follow-up papers to break various things
- Requires memory deduplication or shared libraries
  - Deduplication turned off in Amazon EC2, but available in modern hypervisors
  - Different VMs do not share libraries
- In Linux, shared libraries and deduplication the norm
  - PaaS services vulnerable [Zhang et al. 2014]
Meltdown

- Discovered independently by Jann Horn (Google Project Zero), Cyberus Technology, Graz University

Intel didn’t warn US government about CPU security flaws until they were public

*Meltdown and Spectre were kept secret*

Researchers find malware samples that exploit Meltdown and Spectre

As of Feb. 1, antivirus testing firm AV-TEST had found 139 malware samples that exploit Meltdown and Spectre. Most are not very functional, but that could change.
Meltdown

• Discovered independently by Jann Horn (Google Project Zero), Cyberus Technology, Graz University
• Closely related vulnerability called Spectre
Meltdown

- Read arbitrary kernel and physical-memory locations from unprivileged process

- 503 KB/s!

- Exploits a combination of modern CPU’s use of speculative execution and Flush+Reload
  - Other side-channel attacks can replace F+R
Meltdown: intuition

1  raise_exception();
2  // the line below is never reached
3  access(probe_array[data * 4096]);
Meltdown: design

- Exception Handling/Suppression
  - Transient Instructions
    - Microarchitectural State Change
  - Section 4.1

- Transfer (Covert Channel)
  - Architectural State
  - Section 4.2

- Secret
  - Accessed
  - Leaked

- Recovered Secret
  - Recovery
Meltdown: core spy code

1 ; rcx = kernel address
2 ; rbx = probe array
3 retry:
4 mov al, byte [rcx]
5 shl rax, 0xc
6 jz retry
7 mov rbx, qword [rbx + rax]

Retry reading privileged memory
Access privileged memory
Multiply by page size
Read from an attacker (unprivileged) array at: (secret value) * $2^{12}$
Meltdown: nuances

• Privileged memory access raises segfault
  – Would normally crash process
  – Wrap in TXT or include signal handler
• Race condition between segfault and speculative code
  – Keeping speculative code lightweight helps
  – Some errors will creep up, but not many
• Kernel ALSR can be turned on
  – Won’t know a priori what to set rcx to
  – Can guess and check (8 GB memory requires ~128 guesses)
Meltdown works

503 KB/s using TXT
“exception suppression”

Error rate: 0.02%
Meltdown: countermeasures

• Minimize kernel memory mapped to virtual address space of process
  – KAISER countermeasure for kernel ASLR already deals with this. Suggest immediate deployment
  – Won’t prevent using Meltdown to leak ASLR
• Hard split of virtual memory space into privileged / unprivileged
• Redesign microprocessors
  – Only one that helps with Spectre