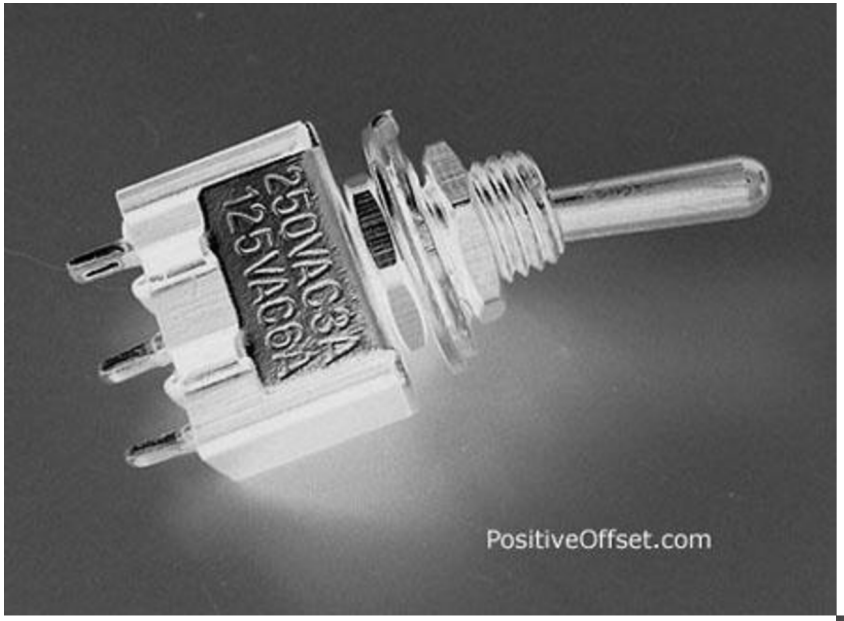
xkcd.com/74/

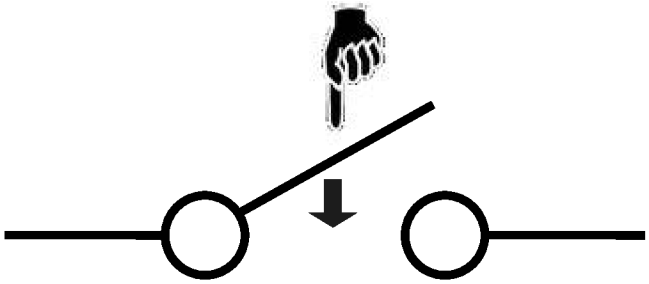
Gates and Logic

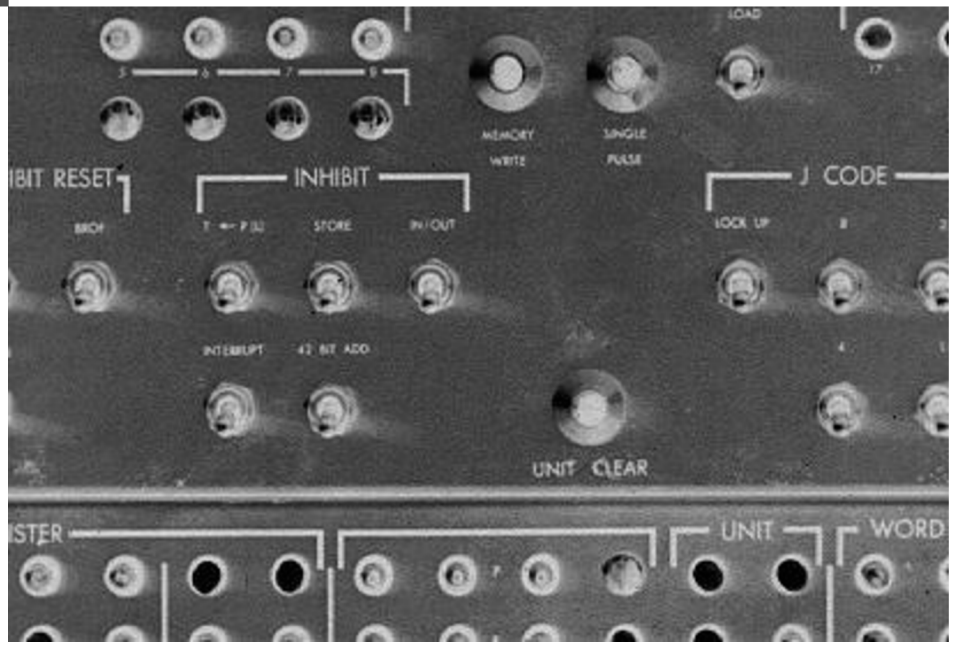
See: P&H Appendix C.2, C.3

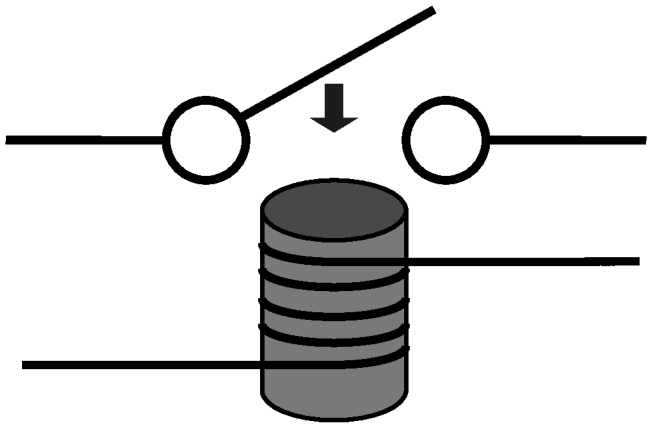


- Acts as a *conductor* or *insulator*

- Can be used to build amazing things…

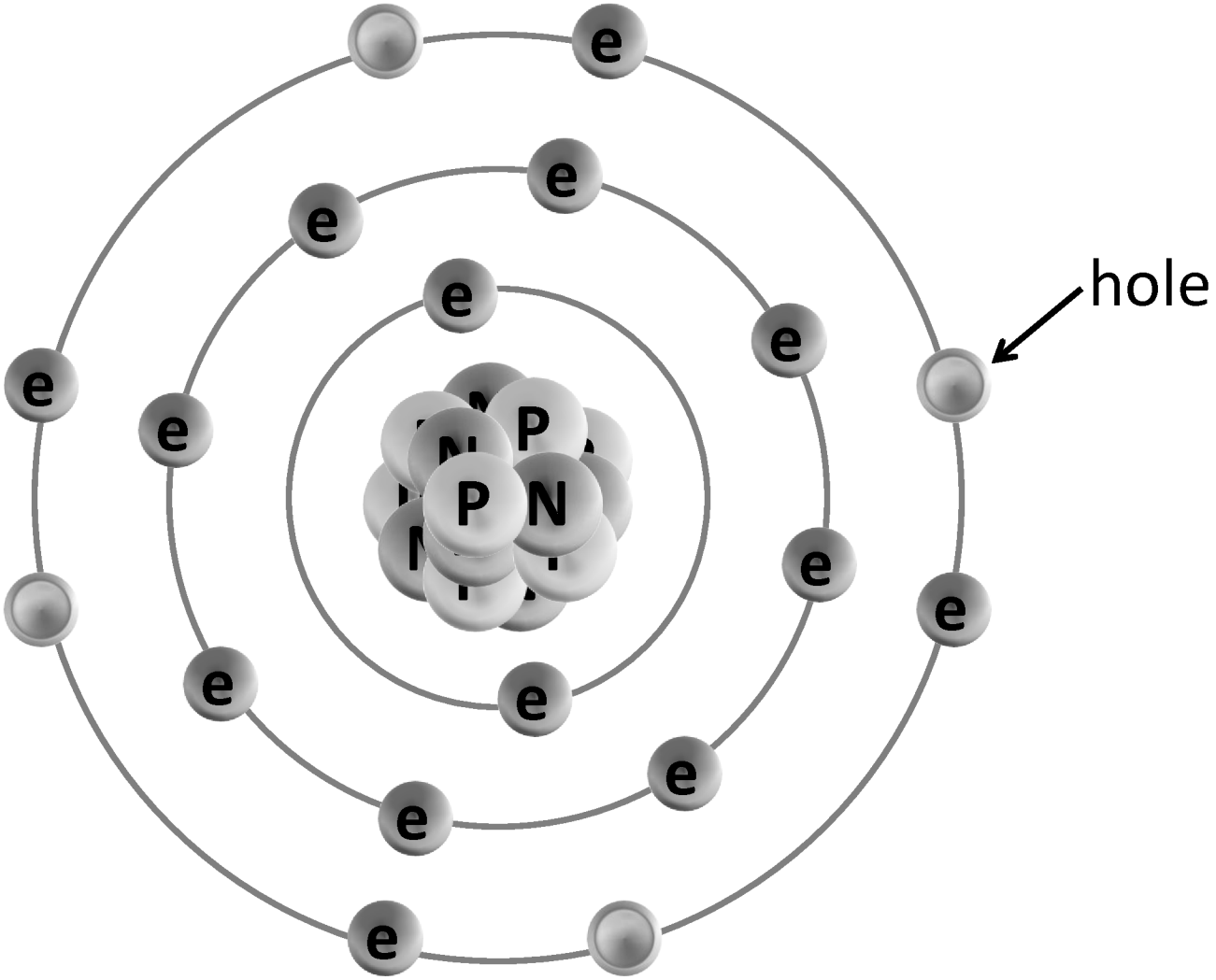


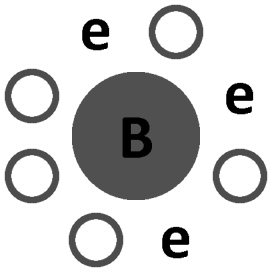




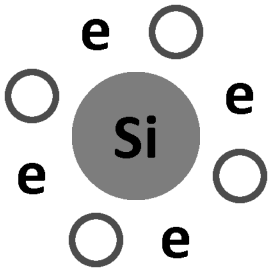
- One current controls another (larger) current

- Static Power:
  - Keeps consuming power when in the *ON* state
- Dynamic Power:
  - Jump in power consumption when switching

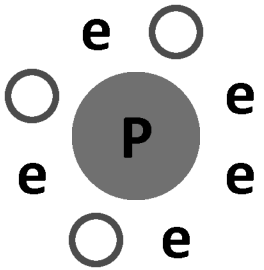

e
P
N
hole



Boron

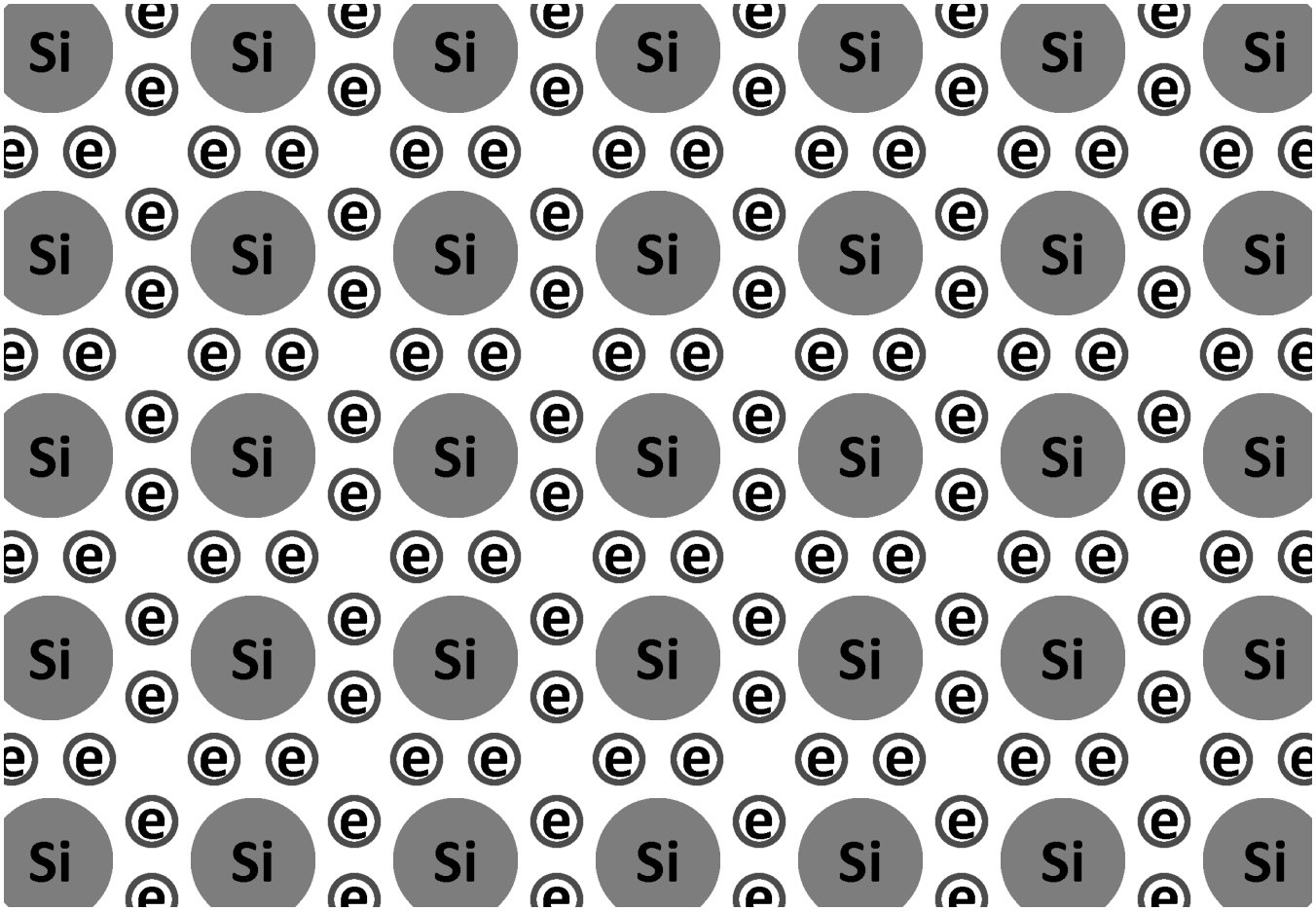


Silicon

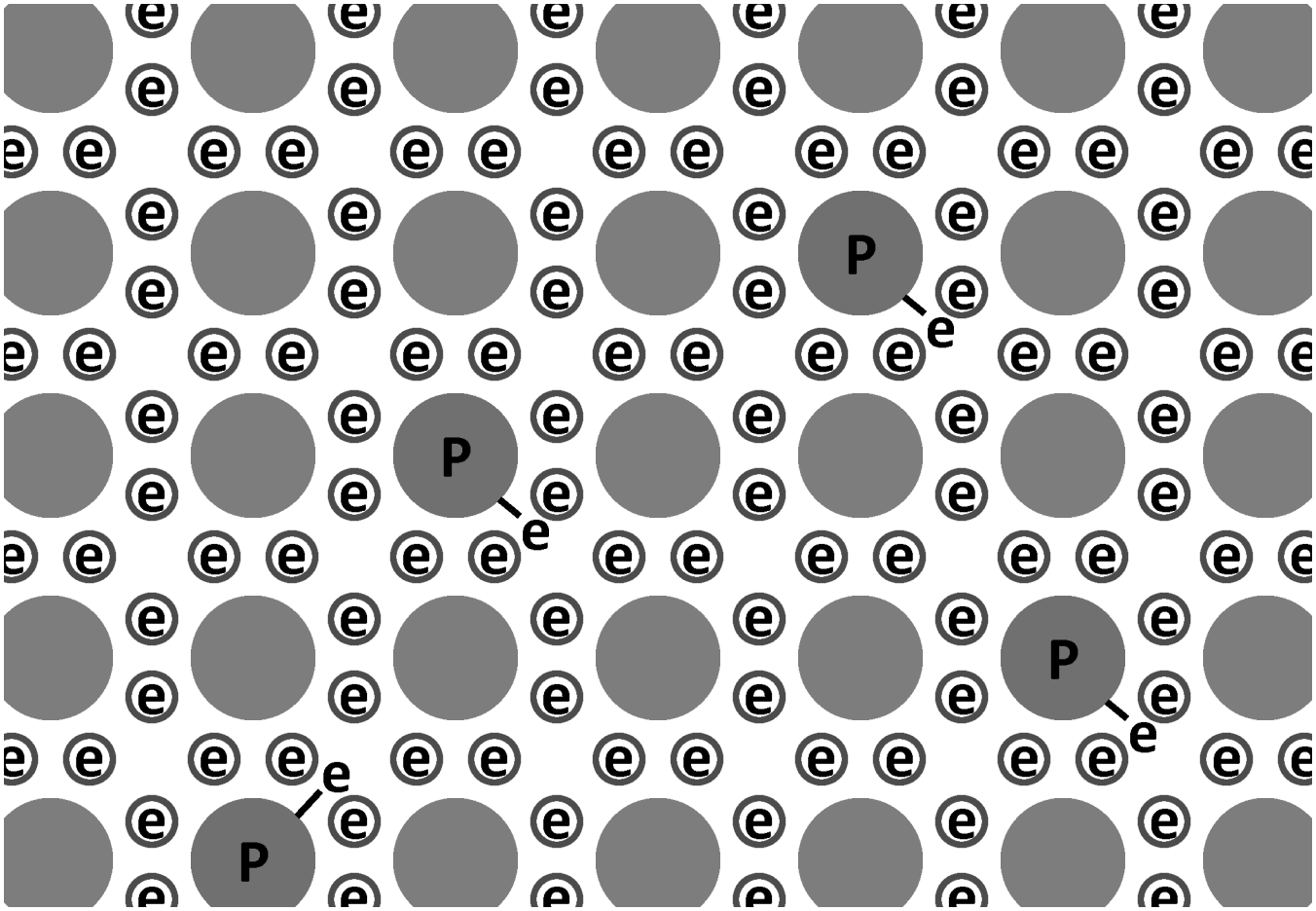


Phosphorus

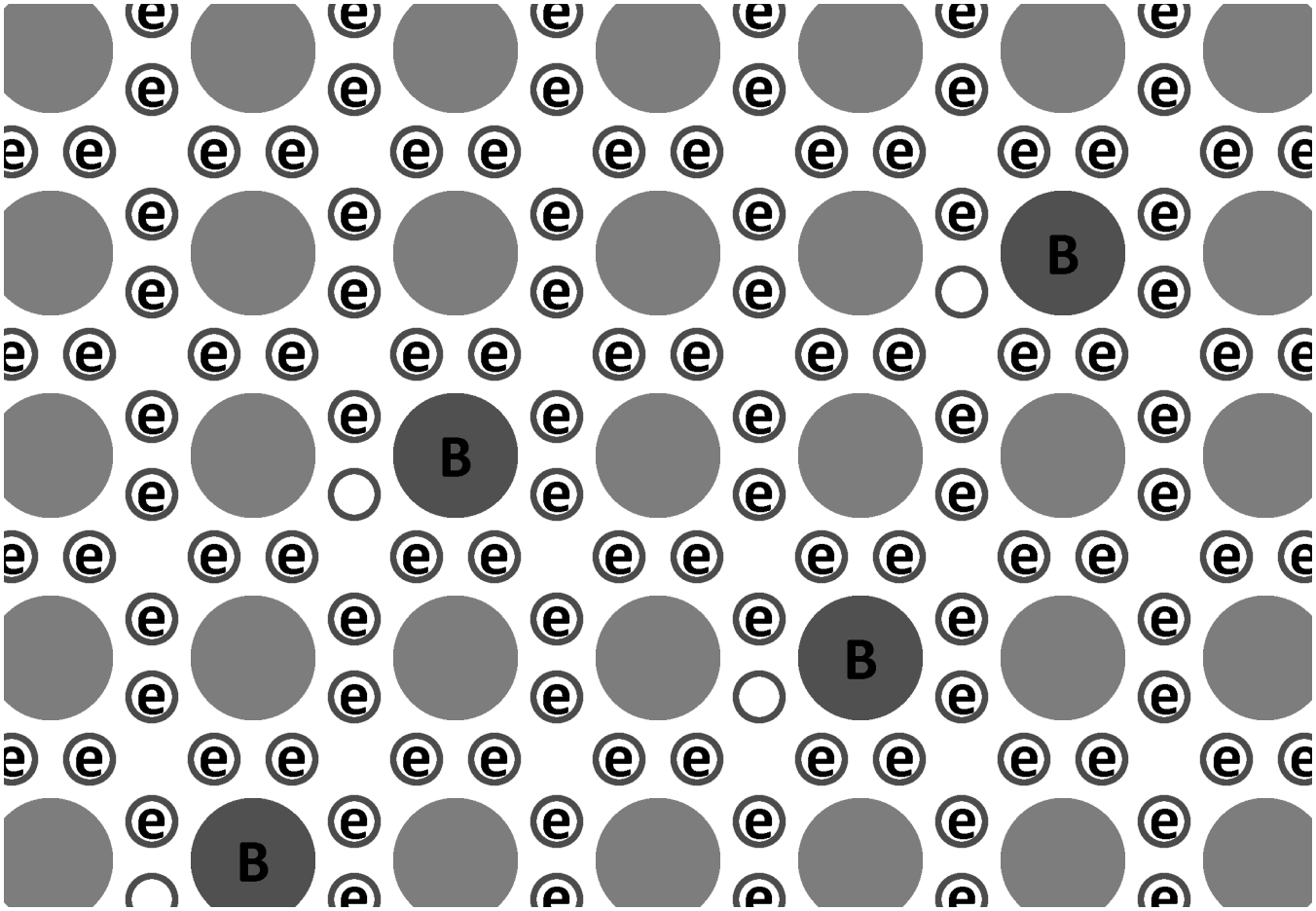
Silicon

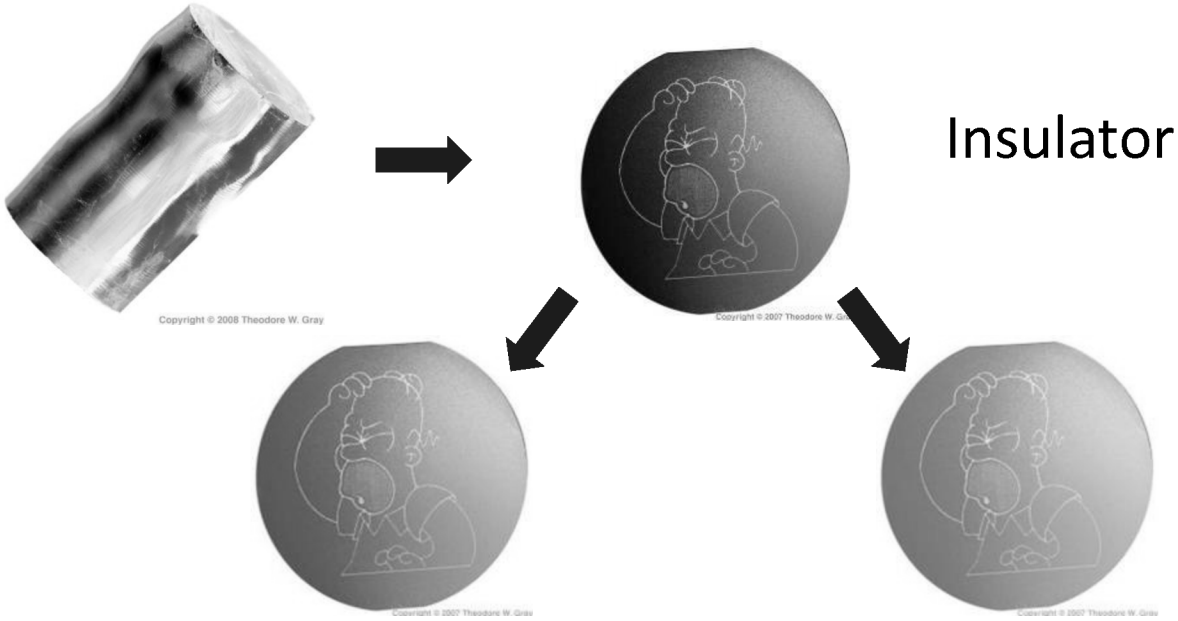


N-Type: Silicon + Phosphorus



P-Type: Silicon + Boron





Insulator

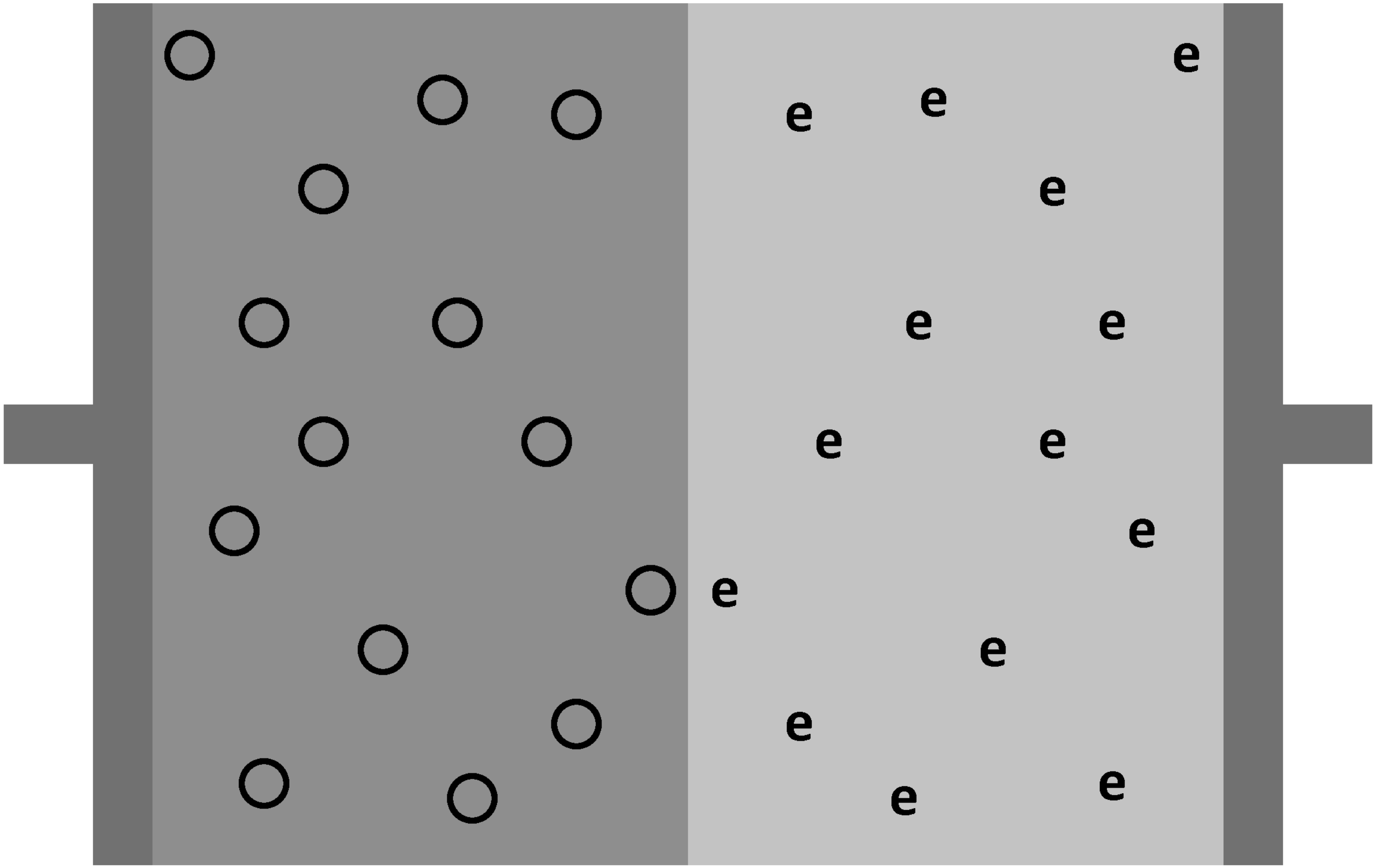
p-type (Si+Boron)
has mobile holes:

low voltage (depleted)
→ insulator
high voltage (mobile holes)
→ conductor

n-type (Si+Phosphorus)
has mobile electrons:

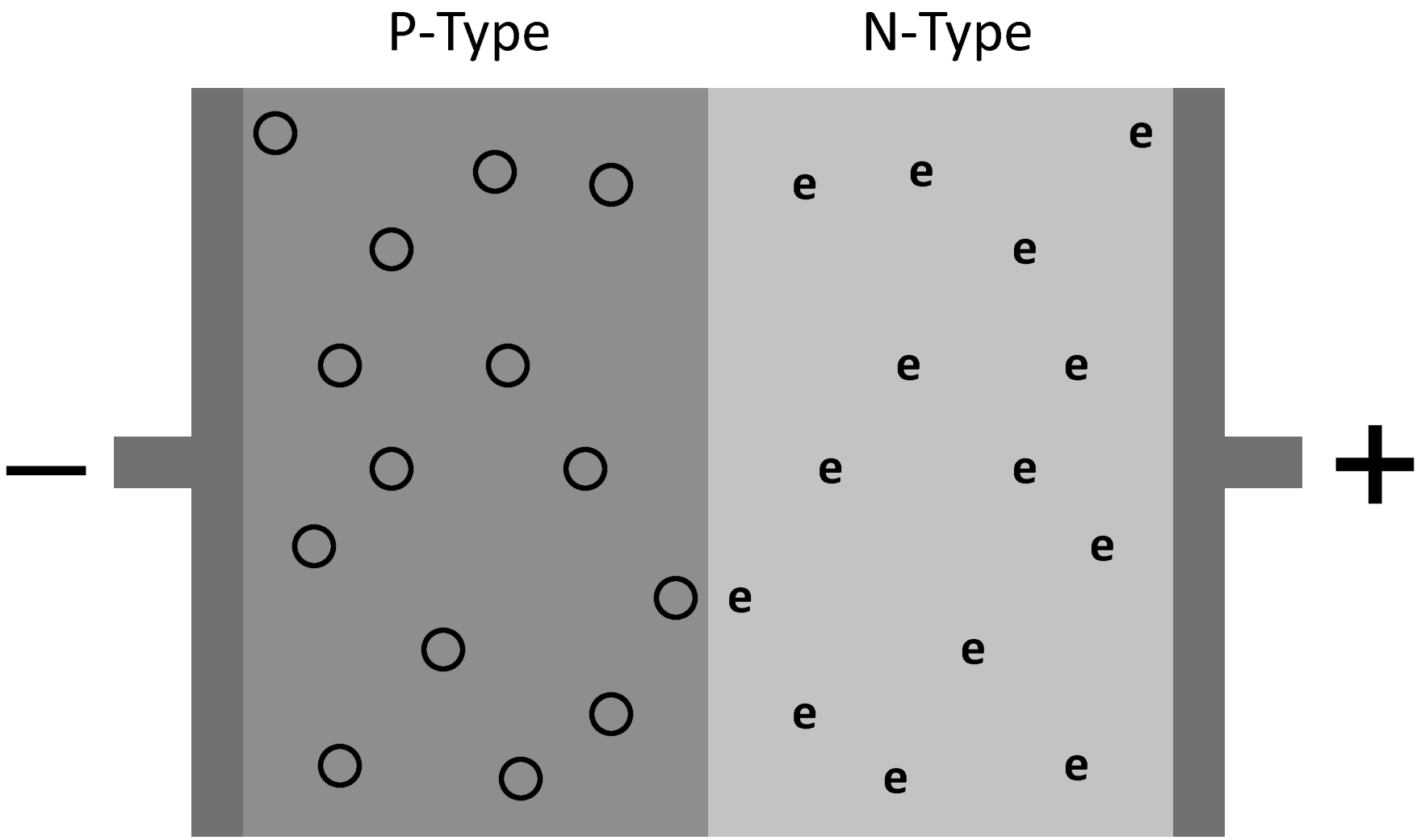
low voltage (mobile electrons)
→ conductor
high voltage (depleted)
→ insulator

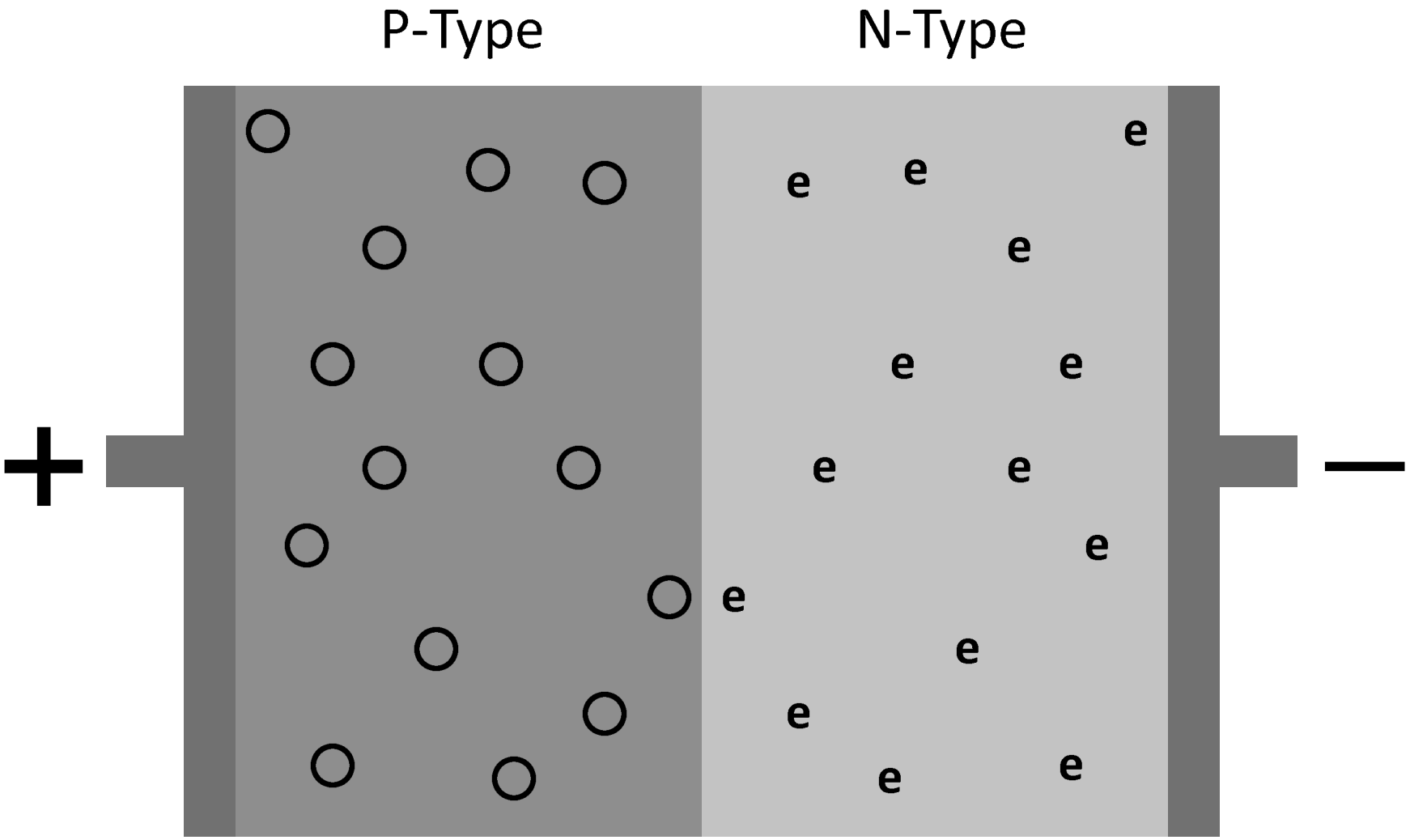
P-Type N-Type



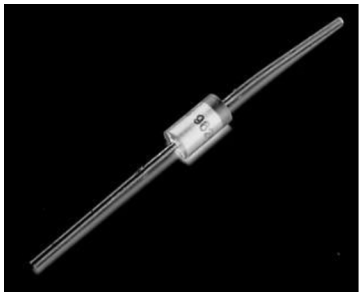
low v → insulator
high v → conductor

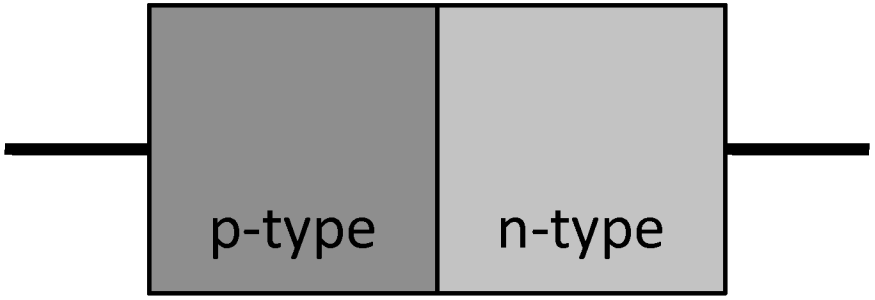
low v → conductor
high v → insulator

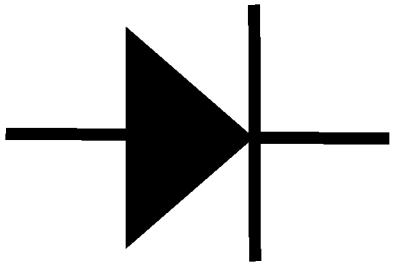

P-Type
N-Type
e
e
e
e
e
e
e
e
e
e
e
e
e
e
e
e
low v → insulator
high v → conductor
low v → conductor
high v → insulator


P-Type
N-Type
+
—
e
e
e
e
e
e
e
e
e
e
e
e
e
e
low v → insulator
high v → conductor
low v → conductor
high v → insulator

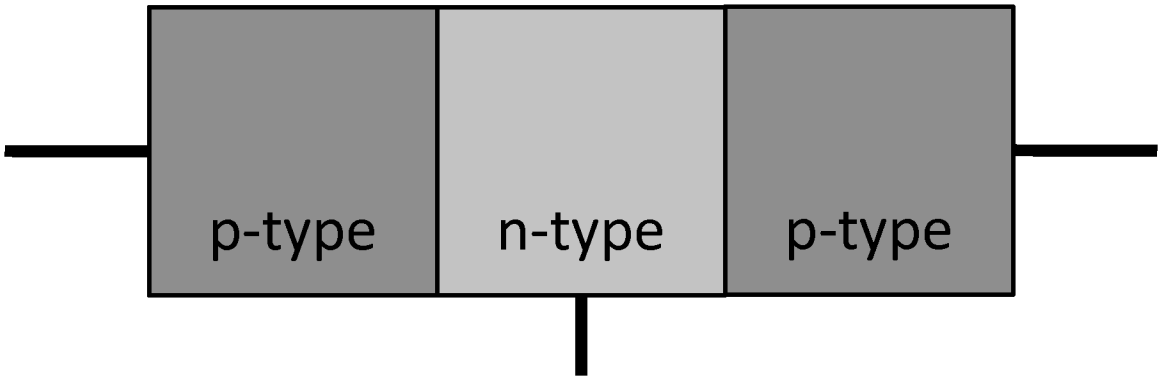
PN Junction “Diode”

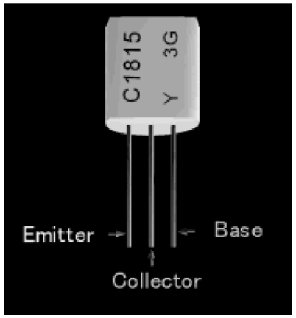






Conventions:
vdd = vcc = +1.2v = +5v = hi
vss = vee = 0v = gnd

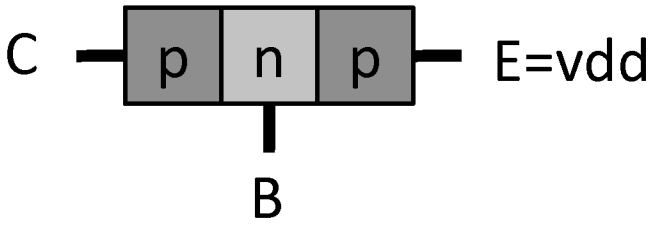

p-type
n-type
p-type



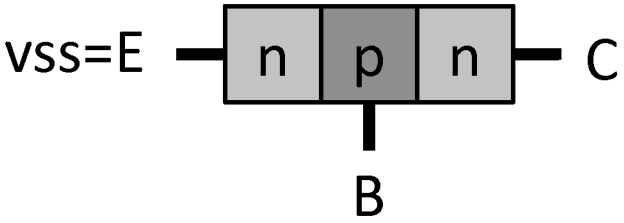
- Solid-state switch: The most amazing invention of the 1900s

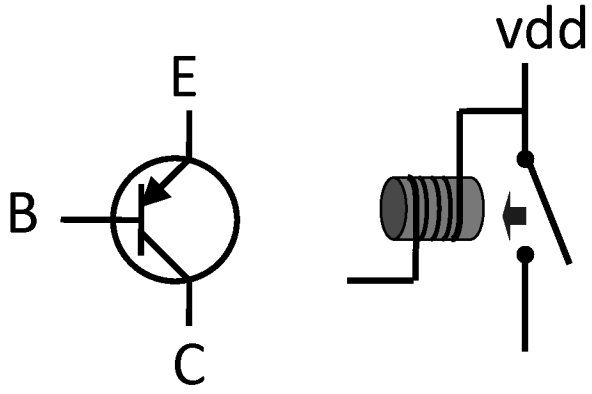
Emitter = “input”, Base = “switch”, Collector = “output”

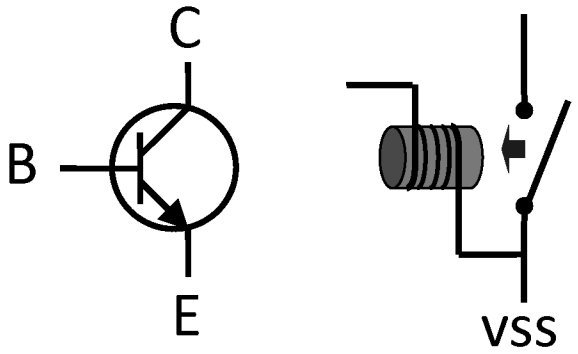
PNP Transistor



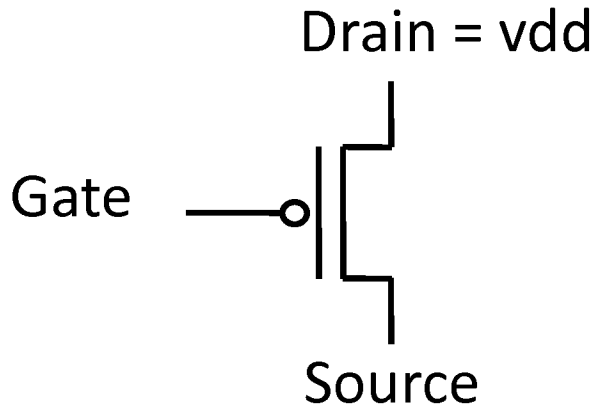
NPN Transistor





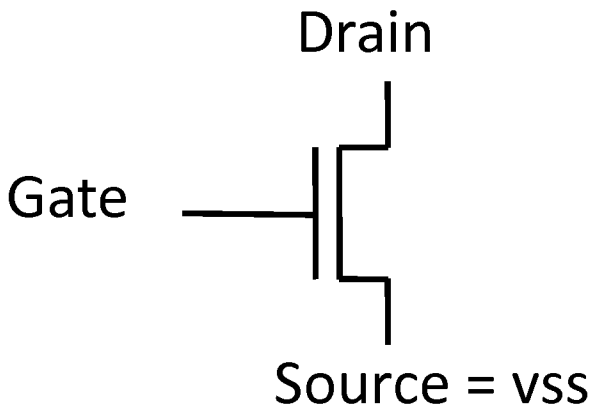


P-type FET

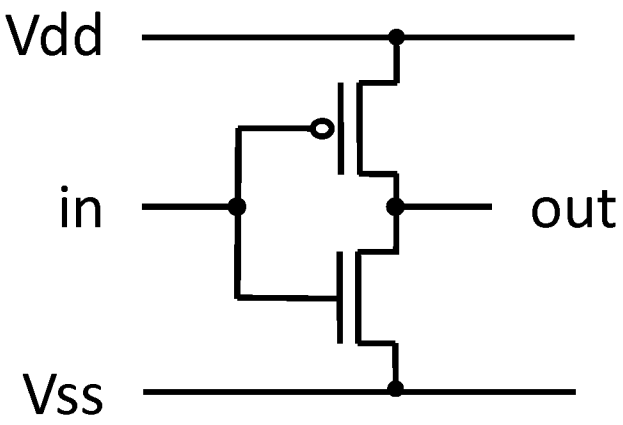


- Connect Source to Drain when Gate = lo
- Drain must be vdd, or connected to source of another P-type transistor

N-type FET

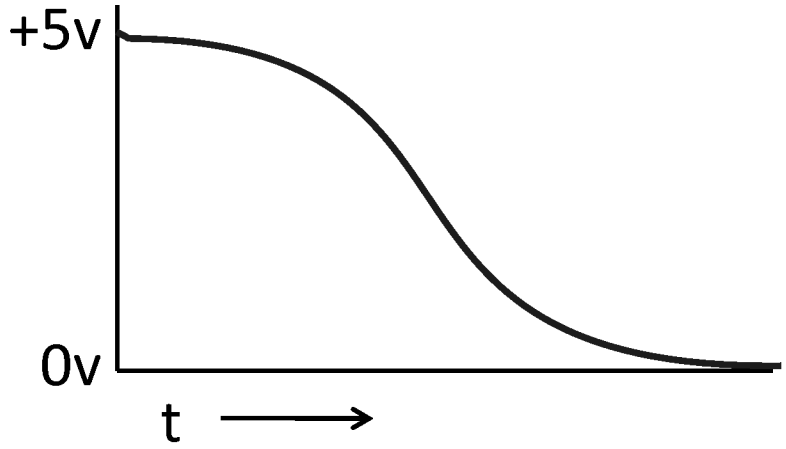


- Connect Source to Drain when Gate = hi
- Source must be vss, or connected to drain of another N-type transistor



In	Out

voltage



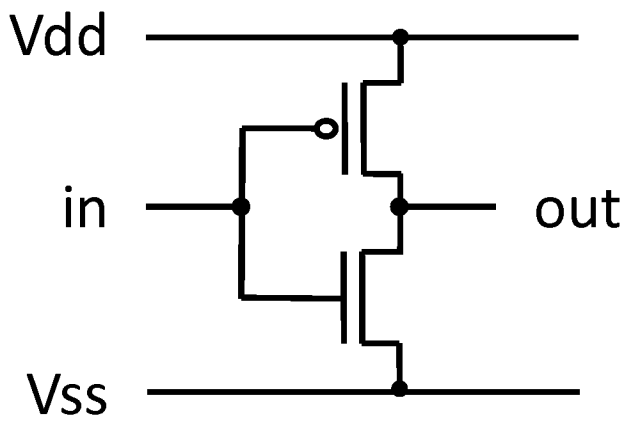
Gate delay

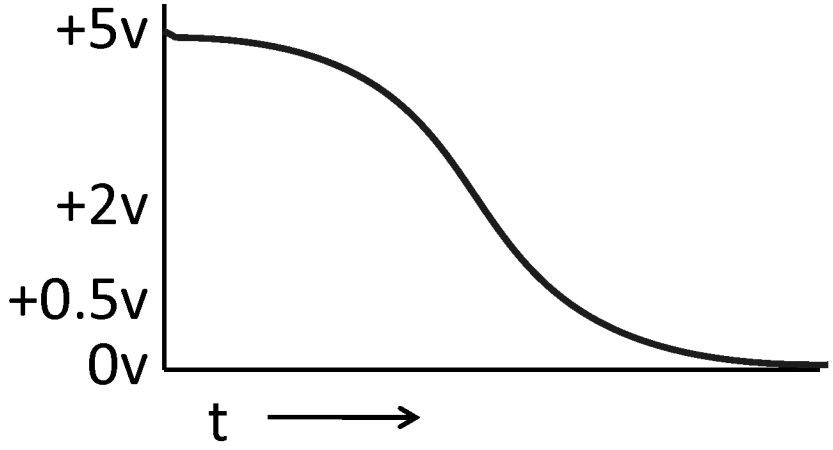
- transistor switching time
- voltage, propagation, fanout, temperature, …

CMOS design

(complementary-symmetry metal–oxide–semiconductor)

- Power consumption = dynamic + leakage





In	Out
+5v	0v
0v	+5v

voltage

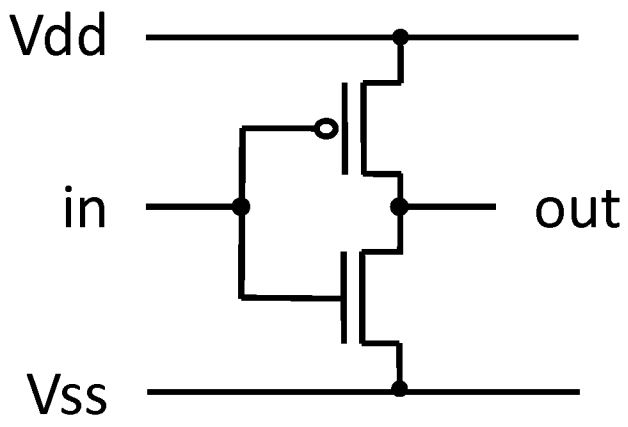
In	Out

truth table

Conventions:

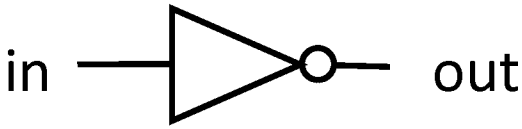
vdd = vcc = +1.2v = +5v = hi = true = 1

vss = vee = 0v = gnd = false = 0



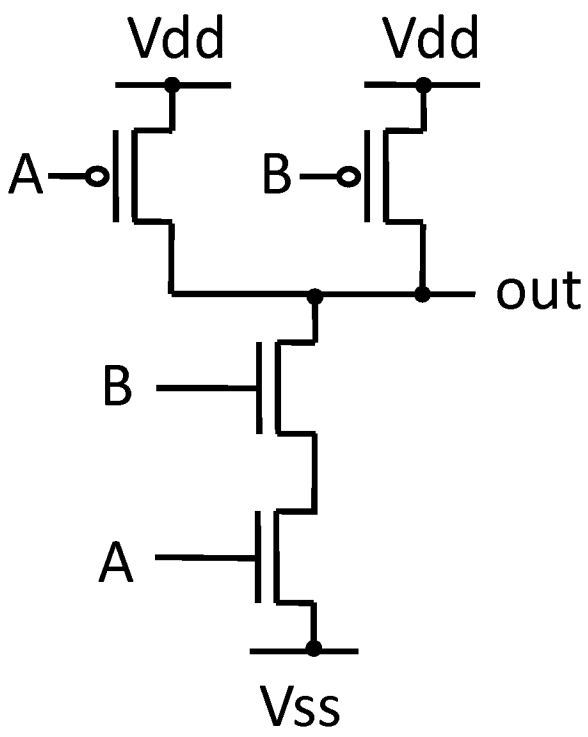
Function: NOT

- Symbol:



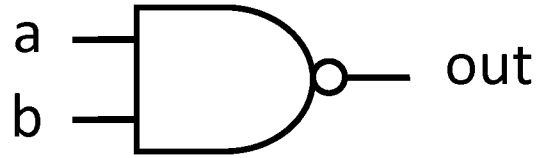
In	Out
0	**1**
1	**0**

Truth table

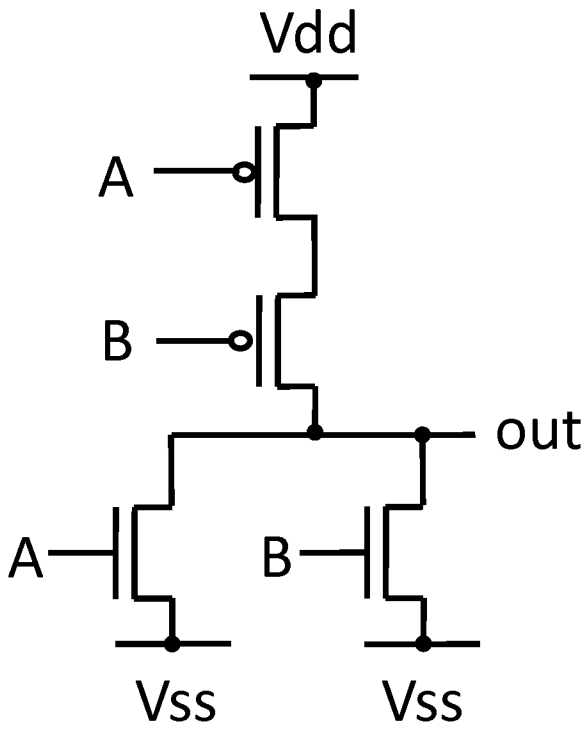


Function: NAND

- Symbol:

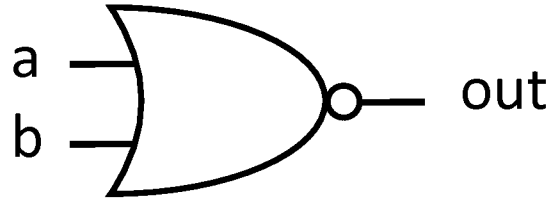


A	B	out
0	0	1
0	1	1
1	0	1
1	1	0

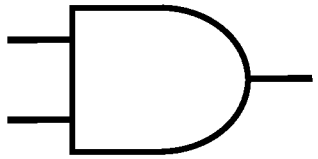
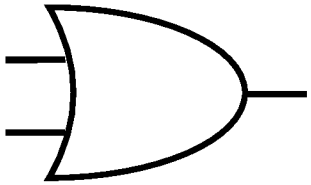
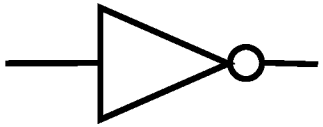


Function: NOR

- Symbol:



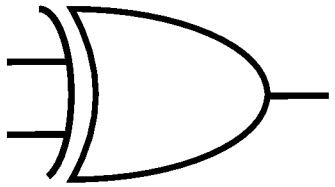
A	B	out
0	0	1
0	1	0
1	0	0
1	1	0

- AND: 
- OR: 
- NOT: 

NAND is universal (so is NOR)

- Can implement any function with just NAND gates
  - De Morgan's laws are helpful (pushing bubbles)
- useful for manufacturing

E.g.: XOR (A, B) = A or B but not both ("exclusive or")



Proof: ?

Some notation:

- constants: true = 1, false = 0
- variables: a, b, out, …
- operators:
  - AND(a, b) = a b = a & b = $a \wedge b$
  - OR(a, b) = a + b = a | b = $a \vee b$
  - NOT(a) = ā = !a = $\neg a$

Identities useful for manipulating logic equations

- For optimization & ease of implementation

$a + 0 = a$

$a + 1 = 1$

$a + \bar{a} = 1$

$a\ 0 = 0$

$a\ 1 = a$

$a\ \bar{a} = 0$

$\overline{(a + b)} = \bar{a}\ \bar{b}$

$\overline{(a\ b)} = \bar{a} + \bar{b}$

$a + a\ b = a$

$a(b+c) = ab + ac$

$\overline{a(b+c)} = \bar{a} + \overline{bc}$

- functions: gates ↔ truth tables ↔ equations
- Example: (a+b)(a+c) = a + bc

a	b	c	a+b	a+c	LHS	bc	RHS
0	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0
0	1	0	1	0	0	0	0
0	1	1	1	1	1	1	1
1	0	0	1	1	1	0	1
1	0	1	1	1	1	0	1
1	1	0	1	1	1	0	1
1	1	1	1	1	1	1	1