CS 316: Arithmetic (contd.)

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Announcements

- Office Hours
  - No recitation this week; instead TAs will hold office hours and discuss

Two's Complement Addition

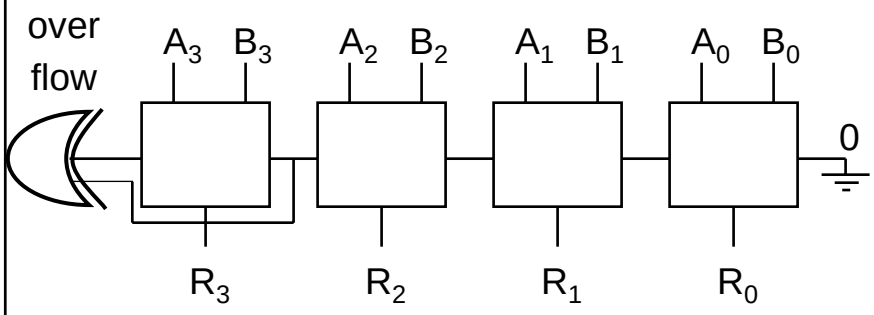
- Perform addition as usual, regardless of sign
  - 1 = 0001, 3 = 0011, 7 = 0111, 0 = 0000
  - -1 = 1111, -3 = 1101, -7 = 1001
- Examples
  - 1 + -1 = 1111 + 0001 = 0000 (0)
  - -3 + -1 = 1111 + 1101 = 1100 (-4)
  - -7 + 3 = 1001 + 0011 = 1100 (-4)

Overflow

- When can it occur?
  - If you add a negative and positive number
    - Cannot occur (Why?)
  - If you add two negatives or two positives
    - Can occur (Why?)
  - Add two positives, and get a negative number
  - Or, add two negatives, get a positive number
    - Overflow!
  - Overflow when
    - Carry into most significant bit (msb) != carry out of msb

Two's Complement Adder

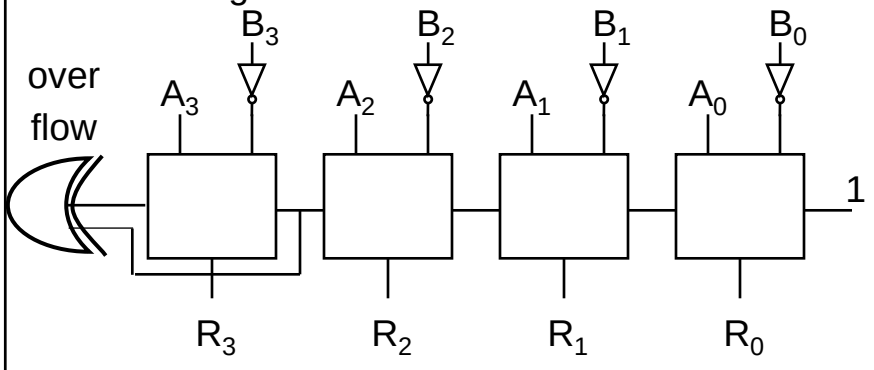
- Let's build a two's complement adder



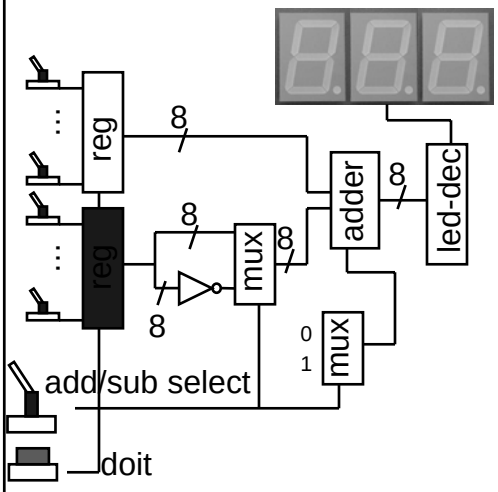
- Already built, just needed to modify overflow checking

Two's Complement Subtraction

- Subtraction is simply addition, where one of the operands has been negated
  - Negation is done by inverting all bits and adding one



A Calculator

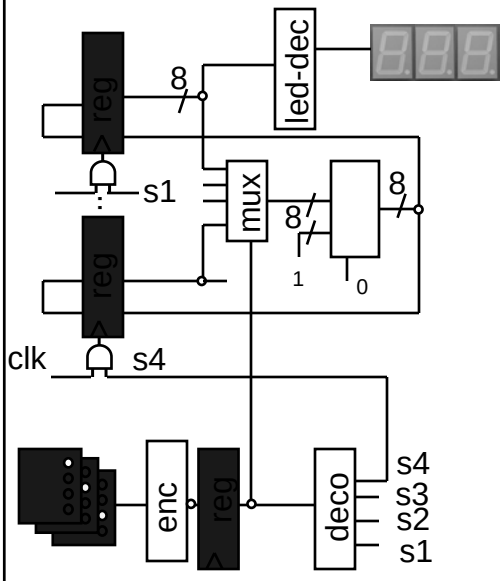


- Enter numbers to be added or subtracted using toggle switches
- Select: ADD or SUBTRACT
- Muxes feed A and B,or A and –B, to the 8-bit adder
- The 8-bit decoder for the hex display is straightforward

Summary

- We can now perform arithmetic
  - And build basic circuits that operate on numbers

A Vote Counter



- Data values flow from set of parallel registers (a register file)
- to the addition unit
- back into the register file

CS 316: Memory

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Register File

- Set of registers
  - Read or written
  - Use register number to access it
- Read or write ports
  - Decoder for each port
- D flip flops to store bits

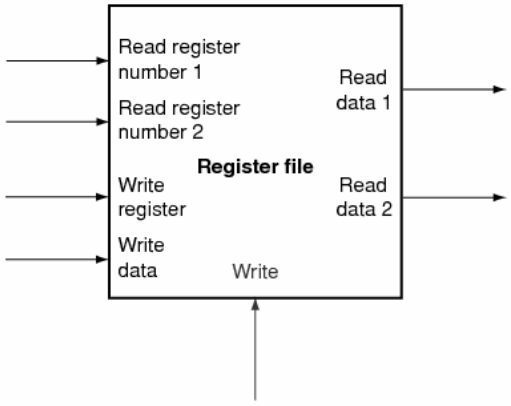
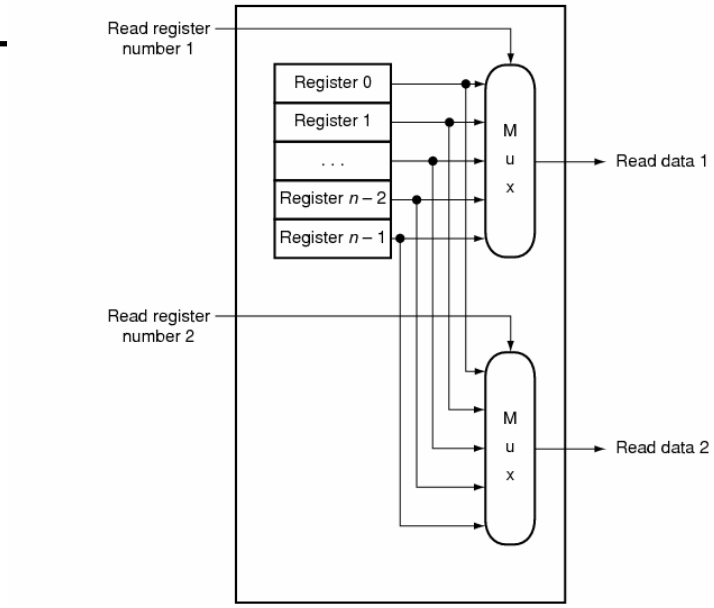


FIGURE B.8.7 A register file with two read ports and one write port has five inputs and two outputs. The control input Write is shown in color.



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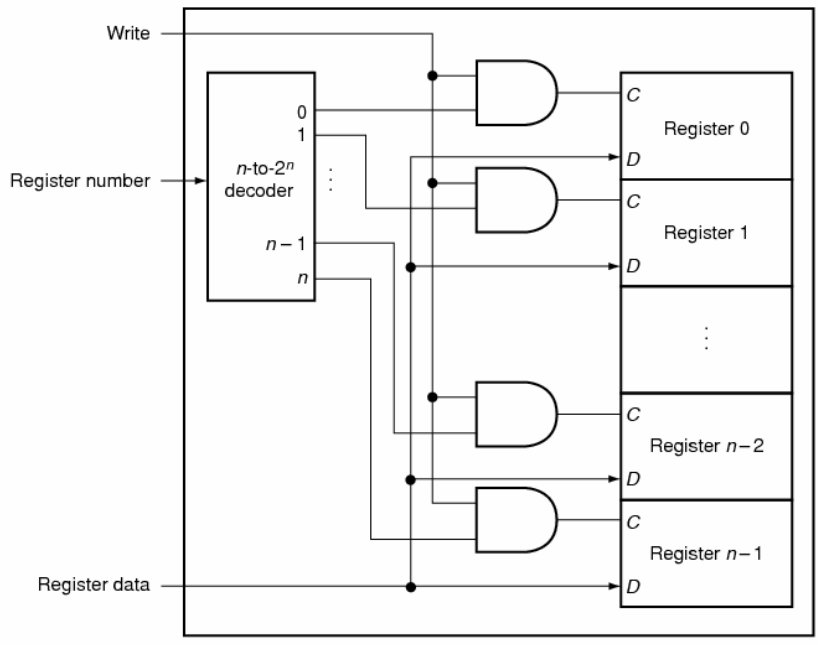

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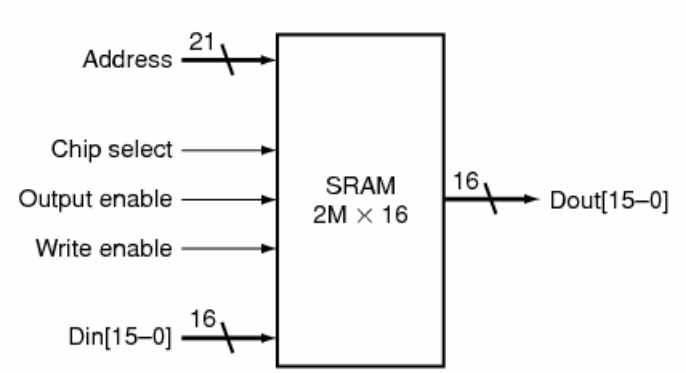
Memory

- Various technologies
  - S-RAM, D-RAM, NV-RAM
- Non-Volatile RAM
  - Data remains valid even through power outages
  - More expensive
  - Limited lifetime; after 100000 to 1M writes, NV-RAM degrades
  - Flash cards

Static RAM: SRAM

- Static-RAM
  - So called because once stored, data values are stable as long as electricity is supplied
  - Based on regular flip-flops with gates



How to build large memories?

- Cannot use a 4M->1 multiplexer!
- Use a shared line (called bit line)
- Multiple memory cells can assert line
  - Need 3 state buffer
  - 3 states: asserted (1), deasserted (0), or high impedance

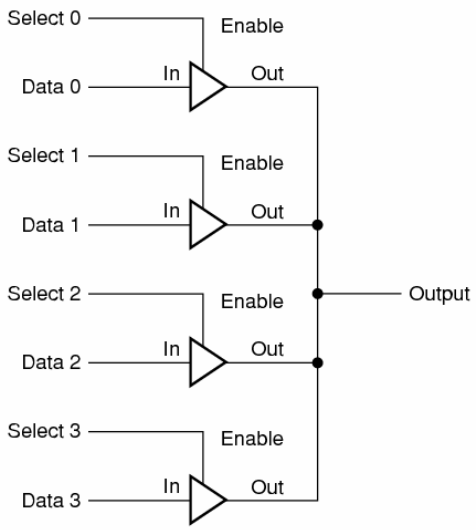


FIGURE B.9.2 Four three-state buffers are used to form a multiplexor. Only one of the four Select inputs can be asserted. A three-state buffer with a deasserted Output enable has a high-impedance output that allows a three-state buffer whose Output enable is asserted to drive the shared output line.

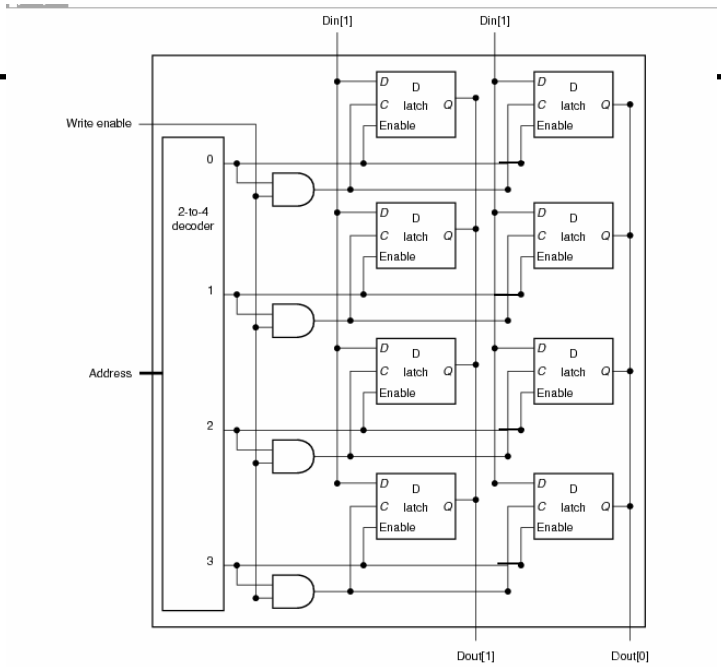


FIGURE B.9.3 The basic structure of a 4 x 2 SRAM consists of a decoder that selects which pair of cells to activate. The acti-

Big Memories

- Tri state buffer got rid of big mux
- But still need a big decoder to pick the right entry
  - 4M x 8 SRAM requires
    - 22 to 4M decoder
    - And 4M lines!
- Instead
  - Rectangular arrays
  - 2-step decode

Parallel Memory Banks

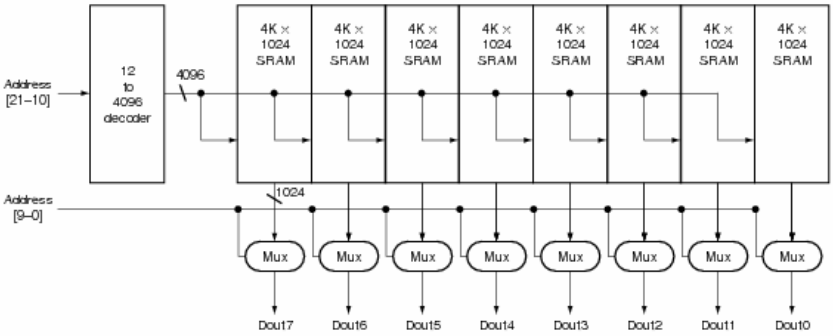


FIGURE B.9.4 Typical organization of a 4M x 8 SRAM as an array of 4K x 1024 arrays. The first decoder generates the addresses for eight 4K × 1024 arrays; then a set of multiplexors is used to select 1 bit from each 1024-bit-wide array. This is a much easier design than a single-level decode that would need either an enormous decoder or a gigantic multiplexor. In practice, a modern SRAM of this size would probably use an even larger number of blocks, each somewhat smaller.

SRAM

- Needs a few gates per cell
- Used for caches (we talk about this later)
- For higher density, use DRAM