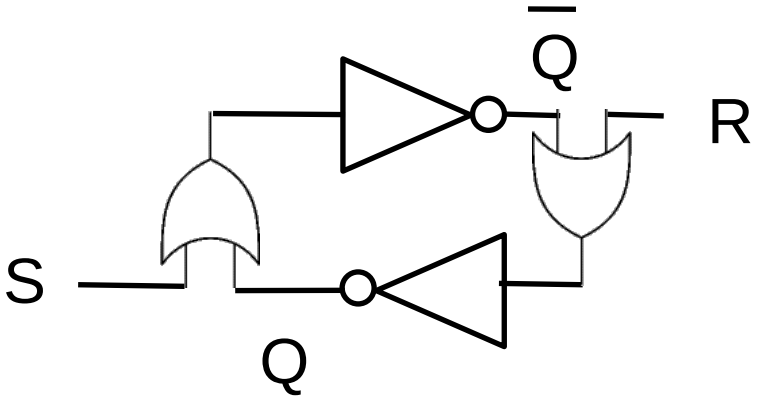
# cs316 section 2: Intro to Logisim + State Machines

- Most real-world hardware design is done using a text-based hardware description language – VHDL, AHDL, etc.
  - Schematics can be "compiled" into a text description
  - Can use a simulator to test the circuit
  - Other back-end tools optimize, perform layout and wire routing, floorplan, etc.
  - Final spec is either downloaded onto a programmable device, or etched into silicon
- We will be using Logisim for all hardware design
  - interactive, graphical schematic editor
  - educational use mainly (makes it user-friendly)

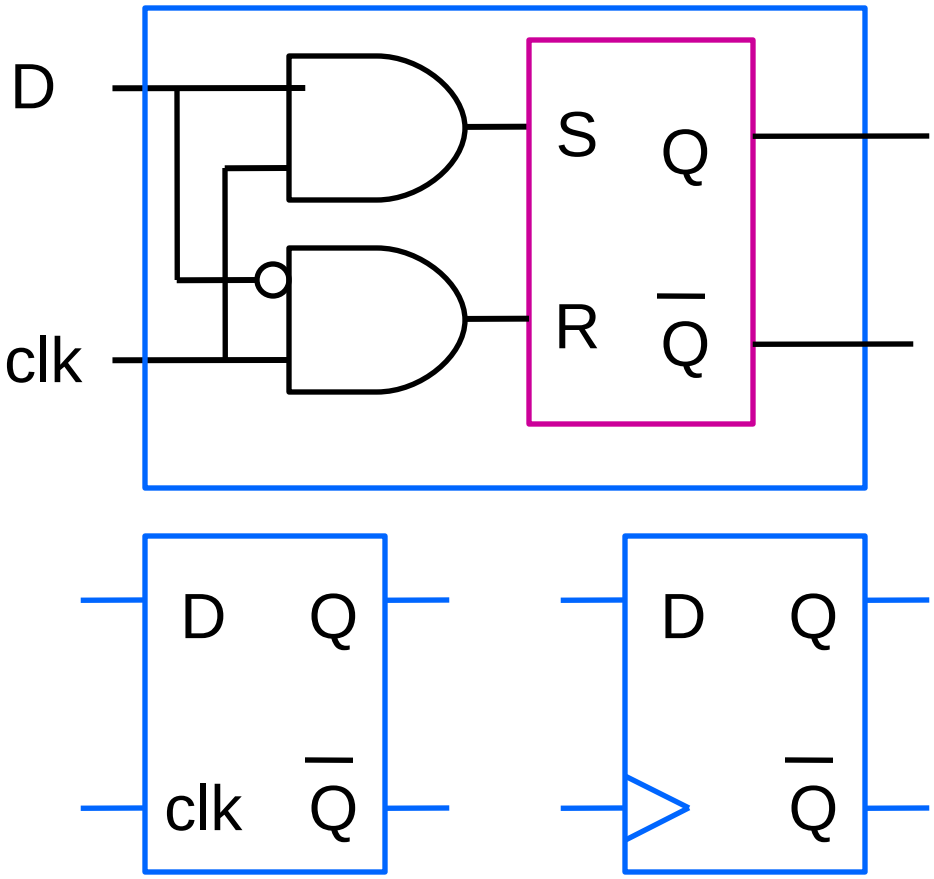
# SR Latch




| S | R | Q | $\overline{Q}$ |
|---|---|---|---|
| 0 | 0 | Q | $\overline{Q}$ |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | ? | ? |

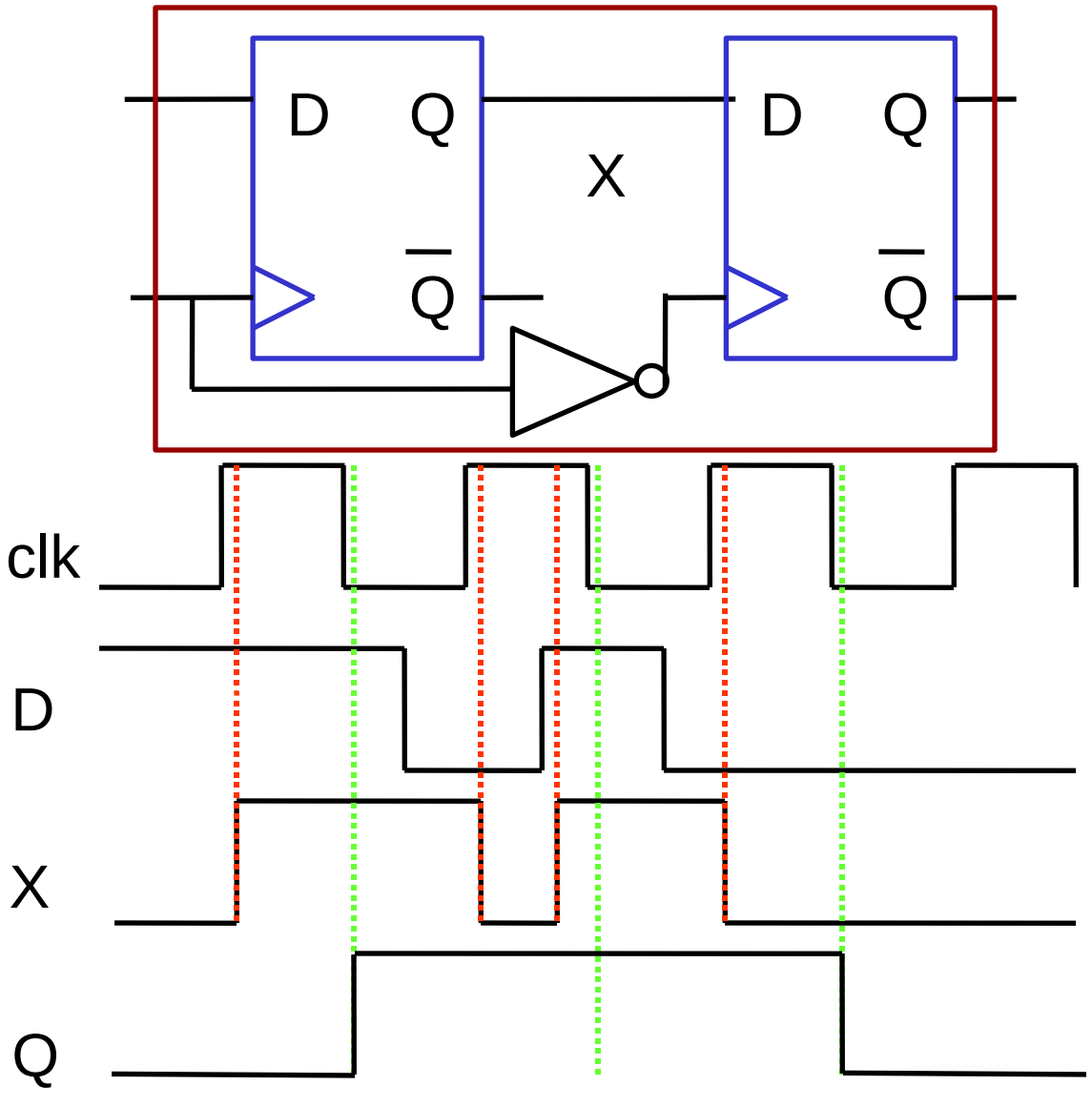
- Set-Reset (S-R) Latch
- Q: Stored value and its complement
- S=1 and R=1 ?

# First Attempt



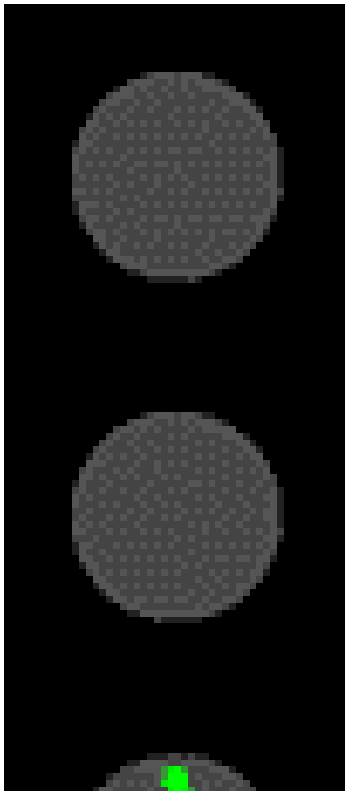

- How does the output behave?

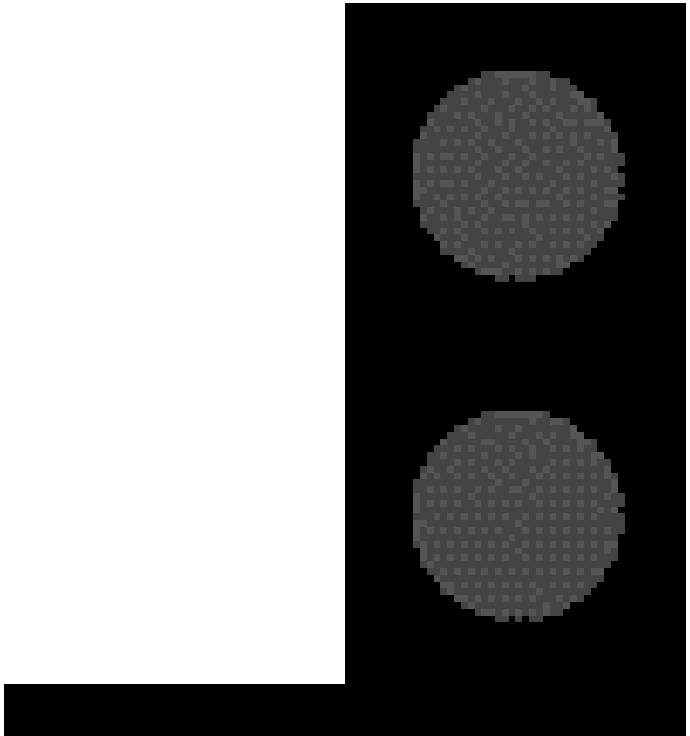
# Master-Slave Flip-Flop

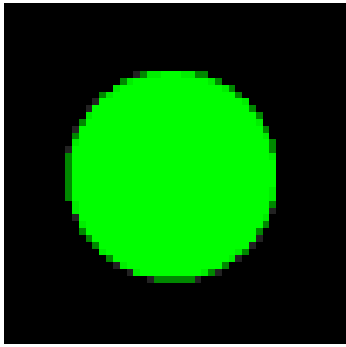



- Outputs change only on falling edges
- Data is captured on rising edges
- Delay in outputs
  - but works out perfectly – data for the next stage is ready half cycle ahead of time

# Traffic Light… ?



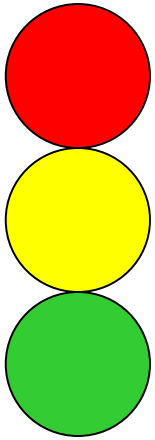




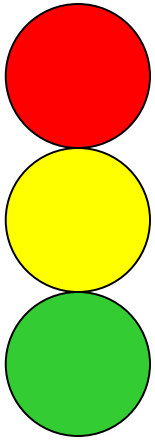
# Simple intersection

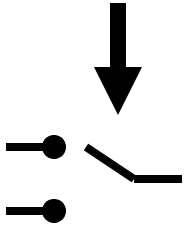
- One non-red light at a time
- Always transition to yellow before red
- Minimum ~10 seconds on green
- ~5 seconds on yellow
- If car sensed at red light
  … then change directions
- Always complete change-of-direction
- Stay green if no cars sensed

NS

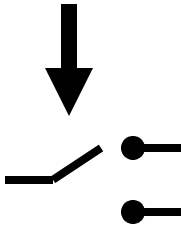


EW





S_NS



S_EW

# Optimize for minimum effort