ECE/CS 314 Fall 2003 **Section 4**

Combinational Logic

From lecture, we have seen the design of a 1-bit full adder. Now, let's try to add a carry-in bit to the input:

A	B	Cin	Sum	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The equations can be derived immediately as:

$$\text{Sum} = \underline{a}\ \underline{b}\ c + \underline{a}\ b\ \underline{c} + a\ \underline{b}\ \underline{c} + a\ b\ c$$
$$\text{Cout} = \underline{a}\ b\ c + a\ \underline{b}\ c + a\ b\ \underline{c} + a\ b\ c$$

To simplify the equations, Karnot Maps should be used:

Sum:

	$\underline{b}\ \underline{c}$	$\underline{b}\ c$	$b\ c$	$b\ \underline{c}$
$\underline{a}$	0	1	0	1
a	1	0	1	0

Cout:

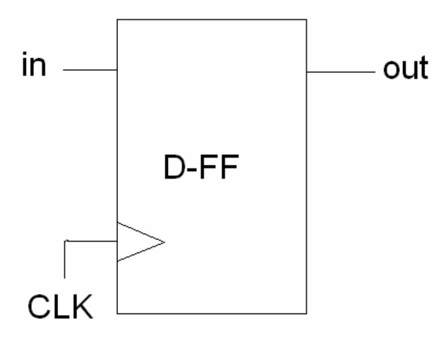
	$\underline{b}\ \underline{c}$	$\underline{b}\ c$	$b\ c$	$b\ \underline{c}$
$\underline{a}$	0	0	1	0
a	0	1	1	1

While Sum cannot be reduced further, Cout can be reduced to:

$$\text{Cout} = a\ c + a\ b + b\ c$$

Sequential Logic

State holding element: D Flip-flop



On a positive edge of the clock signal, the D Flip-flop passes the input value to the output.

Now, let's implement a 2-bit counter:

Reset	S1	S0	S1'	S0'
0	0	0	0	1
0	0	1	1	0
0	1	0	1	1
0	1	1	0	0
1	0	0	0	0
1	0	1	0	0
1	1	0	0	0
1	1	1	0	0

The equations of S0' and S1' can be derived as:

$$S1' = \underline{Reset}\ \underline{S1}\ S0 + \underline{Reset}\ S1\ \underline{S0}$$
$$S0' = \underline{Reset}\ \underline{S1}\ \underline{S0} + \underline{Reset}\ S1\ \underline{S0}$$

And here’s a gate diagram of the circuit: