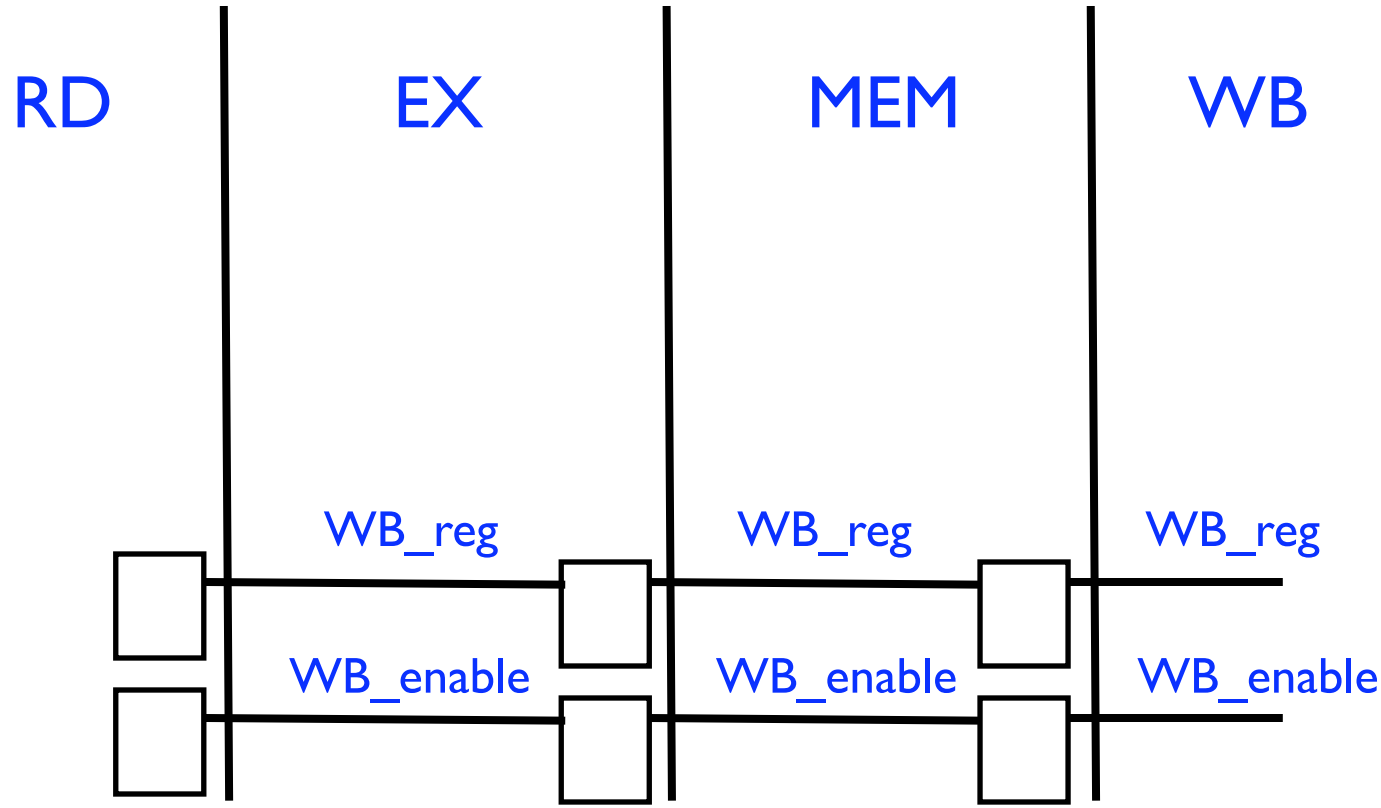
Stuff to be careful about ...

The datapath in the lecture slides does not handle all of the instructions you are required to implement ...

- The immediate field may or may not be sign-extended (xori)
- The link writeback register may or may not be explicit (jal, jalr)
- Computing link value requires the ALU (bgezal, bltazl)
- All memory loads are word-aligned (lb, lh, ...)
  (loaded data may need to be rearranged)
- Bypass must work correctly when writeback register is $0!
  (this is a control logic as well as a datapath issue)
- Next-PC computation is subtle
  (worry about getting delay slots right)

Hints

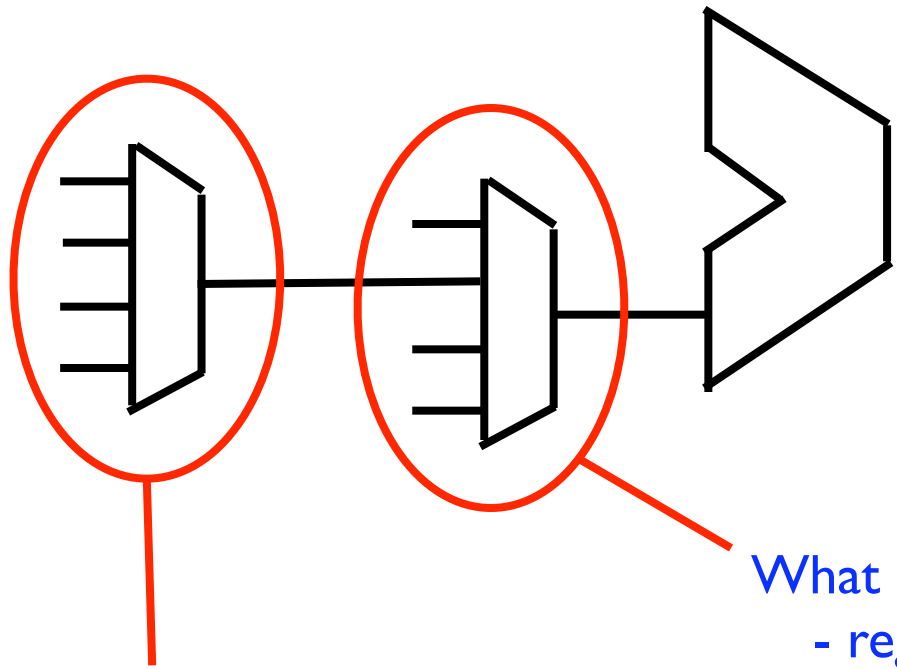
You may want to flop more than just IR,PC between pipeline stages ...



CSL

Hints

Consider a hierarchical arrangement of MUXes on ALU inputs



What kind of input?
- register
- constant
- immediate operand

etc.

Bypassed register value ...
- from register file
- from prev ALU output
- from WB stage

etc.