P4FPGA: Towards an Open Source P4 Backend for FPGA

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Problem Statement
Enable compilation of P4 to many FPGA platforms.

P4FPGA alleviates all of the above problems!

P4FPGA Pipeline
- P4FPGA complements existing software-based process
- Makefile-driven compilation for different target boards

Reference Architecture

Applications
Switch/Router, Intellic-NIC, Packet Scheduling

Status
We have implemented the following components:
- Packet Parser (Fixed parse graph from P4 program)
- Match Table (BCAM)
- Packet Memory (Backed by Block RAM in FPGA)
- Tx/Rx Ring Buffer (Backed by Block RAM)
- Action Engine (Subset of primitivies)
- Control and debug API through PCIe (Gen2)

To be released at p4fpga.org

Workflow

Conclusion
- Open-source compilation framework
- Full system simulation support
- RPC-style SW/HW communication
- Extensible for new data-plane features

Reference
(1) http://www.connectal.org/ (FPGA'15)
(2) Towards Programmable Packet Scheduling (HotNet'15)
(3) Modular SRAM-Based Binary Content-Addressable Memories (FCCM'15)