CS4110

Programming Languages & Logics

Victory Lap!







We've covered a lot of territory this semester...

...now you're ready to soar!

Victory Lap





CS 4110 Home Project Resources Schedule Syllabus CMS Campuswire

Schedule

Date	Topic	Notes
September 2	Course Overview	slides video
September 4	Introduction to Semantics	slides notes video
September 7	Inductive Definitions	<u>slides notes video</u>
September 9	Properties and Inductive Proofs	<u>same slides same notes video</u>
September 11	Inductive Proof and Large-Step Semantics	<u>slides notes video</u>
September 14	The IMP Language	<u>slides notes video</u>
September 16	IMP Properties	<u>slides notes video</u>
September 18	More IMP Proofs	<u>same slides same notes whiteboard-1 whiteboard-2 video-1 video-2</u>
September 21	Denotational Semantics	<u>slides notes video</u>
September 23	Denotational Semantics Examples	<u>slides notes video</u>
September 25	Axiomatic Semantics	<u>slides notes video</u>
September 28	Hoare Logic	<u>slides notes video</u>
September 30	Hoare Logic Examples	<u>slides notes video</u>
October 2	Weakest Preconditions	<u>slides notes video</u>
October 5	λ-Calculus	<u>notes video</u>
October 7	More λ-Calculus and Substitution	<u>slides notes video</u>
October 9	de Bruijn and Combinators	<u>slides notes video</u>
October 12 October 14	Encodings Mid-semester break	<u>slides notes video</u>

October 16	Encodings and Fixed-Point Combinators	<u>slides notes video</u>	
October 19 October 21 October 23	Definitional Translation Continuations Types	<u>slides notes video</u> <u>slides notes video</u> <u>slides notes video</u>	HW4 due
October 26 October 28 October 30	More Types Proving Type Soundness More Proving Type Soundness	<u>same slides same notes video</u> <u>slides notes video</u> <u>same slides same notes video</u>	HW5 due
November 2 November 4 November 6	Normalization Advanced Types Polymorphism	<u>slides notes video</u> <u>slides notes video</u> <u>slides notes video</u>	HW6 due
November 9 November 11 November 13	Type Inference Recursive Types Records and Subtyping	<u>slides notes video</u> <u>slides notes video</u> <u>slides notes video</u>	Take-Home P Project Alpha
November 16 November 18 November 20	Study days Semi-finals Semi-finals		
November 23 November 25 November 27	Semi-finals No class (Thanksgiving) No class (Thanksgiving)		
November 30 December 2 December 4	Existential Types Propositions as Types Dependent Types	<u>slides notes video</u> <u>slides notes video</u> <u>notes video code</u>	Project Beta o
December 7 December 9 December 11	Concurrency Probabilistic Semantics After 4110	<u>slides</u>	Homework 7
December 14 December 16	DSLs and Bidirectional Programming Victory Lap	<u>slides video</u>	Homework 8 Final Project

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September 28	Hoare Logic	slides notes video
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October 2	Weakest Preconditions	slides notes video
October 5	λ-Calculus	notes video
October 7	More 2-Calculus and Substitution	rlider poter video
October 7	de Pruije and Combinators	slides notes video
October 9	de Bruijn and Combinators	sides notes video
October 12	Encodings	slides notes video
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September 16	IMP Properties	slides notes video
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September 21 September 23 September 25	Denotational Semantics Denotational Semantics Examples Axiomatic Semantics	<u>slides notes video</u> <u>slides notes video</u>
September 28 September 30 October 2	Hoare Logic Hoare Logic Examples Weakest Preconditions	<u>slides notes video</u> <u>slides notes video</u> <u>slides notes video</u>
October 5 October 7 October 9	λ-Calculus More λ-Calculus and Substitution de Bruijn and Combinators	<u>notes video</u> <u>slides notes video</u> <u>slides notes video</u>
October 12	Encodings	slides notes video
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October 5	A-Calculus Mars 3. Calculus and Substitution	notes video
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October 23	Types	slides notes video	
October 26	More Types	same slides same notes video	HW5 due
October 28	Proving Type Soundness	slides notes video	
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November 2	Normalization	slides notes video	HW6 due
November 4	Advanced Types	slides notes video	
November 6	Polymorphism	slides notes video	
November 9	Type Inference	slides notes video	Take-Home P
November 11	Recursive Types	slides notes video	
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November 30	Existential Types	slides notes video	
December 2	Propositions as Types	slides notes video	
December 4	Dependent Types	notes video code	Project Beta
December 7	Concurrency	slides video	Homework 7
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September 4	Introducti Mathiam	atical Proliminarias	
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September 9	Properties and Inductive Proofs	same slides same notes video	
September 11	Inductive Proof and Large-Step	Semantics slides notes video	
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September 16	IMP Properties	slides notes video	
September 18	More IMP Proofs	same slides same notes whiteboard-1 v	whiteboard-2 video-1 video-2
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September 25	Axiomatic Semantics	slides notes video	
September 28	Hoare Logic	slides notes video	
September 30	Hoare Logic Examp	matic Semantics	
October 2	Weakest Preconditions	slides notes video	
October 5	λ-Calculus	notes video	
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October 9	de Bruijn and Combinators	N-Calculus	
October 12	Encodings	slides notes video	
October 14	Mid-semester break		

OCIDOBL 16	Encodings and Fixed-Point Com	inators sides note ideo	
October 19	Definitional Translation	alculus programming	HW4 due
October 21	Continuations	slides notes video	
October 23	Types	<u>slides notes video</u>	
October 26	More Types	 same slides same notes video 	HW5 due
October 28	Proving Type Soundness	Simple lypes	
October 30	More Proving Type Soundness	same si des same notes video	
November 2	Normalization	<u>slides notes video</u>	HW6 due
November 4	Advanced Types	slides notes video	
November 6	Polymorphism	slides notes video	
November 9	Type Inference	Advanced lypes	Take-Home P
November 11	Recursive Types	slides notes video	
November 13	Records and Subtyping	<u>slides notes video</u>	Project Alpha
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CS 4110 Home Project Resources Schedule Syllabus CMS Campuswire

Schedule

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September 11	Inductive Proof and Large-Step Semantics	<u>slides notes video</u>
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September 18	More IMP Proofs	same slides same notes whiteboard-1 whiteboard-2 video-1 video-2
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October 12	Encodings	<u>slides notes video</u>
October 14	Mid-semester break	



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October 26	More Types	 same slides same notes video 	HW5 due
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October 14	Mid-semester break	



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Interpreters



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Interpreters Verifiers



Trend: Verified Software

- Researchers are increasingly developing operational models of real-world languages
- Progress in verification makes it possible to build end-to-end verified systems
- Example: CompCert
- Formal semantics for (a large subset of C)
- Formal semantics for PPC (and later x86)
- Full compiler verified in Coq



DOI:10.1145/1538788.1538814

Formal Verification of a Realistic Compiler

By Xavier Leroy

Abstract

This paper reports on the development and formal verification (proof of semantic preservation) of CompCert, a compiler from Clight (a large subset of the C programming language) to PowerPC assembly code, using the Coq proof assistant both for programming the compiler and for proving its correctness. Such a verified compiler is useful in the context of critical software and its formal verification: the verification of the compiler guarantees that the safety properties proved on the source code hold for the executable compiled code as well.

1. INTRODUCTION

Can you trust your compiler? Compilers are generally assumed to be semantically transparent: the compiled code should behave as prescribed by the semantics of the source program. Yet, compilers—and especially optimizing compilers—are complex programs that perform complicated symbolic transformations. Despite intensive testing, bugs in compilers do occur, causing the compilers to crash at compile-time or—much worse—to silently generate an incorrect executable for a correct source program.

For low-assurance software, validated only by testing, the impact of compiler bugs is low: what is tested is the executable code produced by the compiler; rigorous testing should expose compiler-introduced errors along with errors already present in the source program. Note, however, that compiler-introduced bugs are notoriously difficult to expose and track down. The picture changes dramatically for safetycritical, high-assurance software. Here, validation by testing reaches its limits and needs to be complemented or

preserves the semantics of the source programs. For the last 5 years, we have been working on the development of a real*istic, verified* compiler called CompCert. By *verified*, we mean a compiler that is accompanied by a machine-checked proof of a semantic preservation property: the generated machine code behaves as prescribed by the semantics of the source program. By *realistic*, we mean a compiler that could realistically be used in the context of production of critical software. Namely, it compiles a language commonly used for critical embedded software: neither Java nor ML nor assembly code, but a large subset of the C language. It produces code for a processor commonly used in embedded systems: we chose the PowerPC because it is popular in avionics. Finally, the compiler must generate code that is efficient enough and compact enough to fit the requirements of critical embedded systems. This implies a multipass compiler that features good register allocation and some basic optimizations.

Proving the correctness of a compiler is by no ways a new idea: the first such proof was published in 1967¹⁶ (for the compilation of arithmetic expressions down to stack machine code) and mechanically verified in 1972.¹⁷ Since then, many other proofs have been conducted, ranging from single-pass compilers for toy languages to sophisticated code optimizations.⁸ In the CompCert experiment, we carry this line of work all the way to end-to-end verification of a complete compilation chain from a structured imperative language down to assembly code through eight intermediate languages. While conducting the verification of CompCert, we found that many of the nonoptimizing translations performed, while often considered obvious in the compiler literature, are surprisingly tricky to formally prove correct.

This paper gives a high-level overview of the CompCert



Petr4: Formal Foundations for P4 Data Planes

RYAN DOENGES, Cornell University, USA MINA TAHMASBI ARASHLOO, Cornell University, USA ALEXANDER CHANG, Cornell University, USA NEWTON NI, Cornell University, USA SAMWISE PARKINSON, Cornell University, USA RUDY PETERSON, Cornell University, USA ALAIA SOLKO-BRESLIN, Cornell University, USA AMANDA XU, Cornell University, USA

P4 is a domain-specific language for specifying the behavior of packet-processing systems. It is based on an elegant design with high-level abstractions, such as parsers and match-action pipelines, which can be compiled to efficient implementations in hardware or software. Unfortunately, like many industrial languages, P4 lacks a formal foundation. The P4 specification is a 160-page document with a mixture of informal prose, graphical diagrams, and pseudocode. The reference compiler is complex, running to over 40KLoC of C++ code. Clearly neither of these artifacts is suitable for formal reasoning.

This paper presents a new framework, called PETR4, that puts P4 on a solid foundation. PETR4 uses standard elements of the semantics engineering toolkit, namely type systems and operational semantics, to build a compositional semantics that assigns an unambiguous meaning to every P4 program. PETR4 is implemented as an OCaml prototype that has been validated against a suite of over 750 tests from the reference implementation. While developing PETR4, we discovered dozens of bugs in the language specification and the reference implementation, many of which have been fixed. Furthermore, we have used PETR4 to establish the soundness of P4's type system, prove key properties such as termination, and formalize a language extension.





The Petr4 Team







Alexander Chang

Newton Ni



Amanda Xu

Nate Foster





























implements monitoring, etc.

Data plane: forward packets, balances load,



Control Plane: discovers topology, computes routes, enforces policies, etc.



Network Devices: implement packet processing, buffering, queueing, etc. at line rate

Network Programming Challenges







Networks are expected to offer good performance with limited resources

Networks are *distributed* systems with thousands of interacting nodes

Networks enforce complex *security* policies that span trust boundaries

Brief History of Network Verification

On Static Reachability Analysis of IP Networks Geoffrey G. Xie^{*} Jibin Zhan[†] David A. Maltz[†] Hui Zha Albert Greenberg[†] Gisli Hjalmtysson[‡] Jennifer Rexford Hui Zhang[†] ABSTRACT The primary purpose of a network is to provide reachability between applications running on end hosts, this paper, we describe how to compute the reachability a network provides from as anapshot of the configuration of the protecting is the process definition of the protecting is according to the protecting the reactive closure of the influence of packet transformations (e.g., by NATs of reachability soft is influence of packet transformations (e.g., by NATs of reachability is analysis of network reachability is valuable for verify: "analysis of network reachability is valuable for verify: "analysis of network reachability is analysis of network reachability is valuable for verify: "analysis of network reachability is analysis of network reachability is valuable for verify: "analysis of network reachability is analysis of Index Terms- Routing, Static Configuration Analysis. Index Terms- Routing, Static Configuration Analysis. INTRODUCTION While the ultimate goal of networking is to enable communication between hosts that are not directly connected, a wide variety of mechanisms are being used to *limit* the set of destinations the hosts can reach. For example, back bone networks may provide Virtual Private Networks exercise to connect only remote offices belonging to the same enterprise, and enterprise networks themselves are often segmented into departments or offices whose hosts mus to be isolated for business or security reasons. Also, due ta configuration or design mistake, two hosts may notice to the ability to determine a description of the set of the I. INTRODUCTION

segmented into departments or othces whose hosts must work is available. State analysis in an unity availages be isolated for business or security reasons. Also, due to configuration or design mistake, two hosts may not be a configuration or design mistake, two hosts may not be the ability to determine a description of the set of a computation of congarination (in the second of the con-able to communicate under certain failure scenarios, even though the network remains connected; knowing when these vulnerabilities exist is crucial to building a more re-liable network. Research sponsored by the NSF under ANL-0085920, ANL-0331653, ANL-0114014. Views and conclusions contained in this document those of the authors.

and ANYOT NOT A TYPES and Contrained in the document are those of the authors. "Naval Postgraduate School. xie@nps.edu. This work was done while G. G. Xie was a visiting scientist II Carnegie Mellon University. "Carnegie Mellon University. [jibin,dmaltz,hzhang]@cs.cmu.edu "Carnegie Mellon University, Information and Carnegie Mellon University, Information and Carnegie Art. Com. #AT&T Labs-Research. [[albert,gisli,jrex]]@research.att.com. G. Hjalmtysson is also with Reykjavik University.

packets that could traverse the network from a given starting point to a given ending point, whereas expe

ity along the path currently selected by the routing

The ability to evaluate the reachability of a net-work during its *design phase*—before the network



1 Introduction

 Introduction
 In conjugue correctly, we can be comment mataration on slice (e.g. a VLAN) cannot leak into another. This is useful for security, and to help answer questions such as "Can I prevent Host A from talking to Host B?". For example, imagine two health-care providers using
 In the beginning, a switch or router was breathtak-ingly simple. About all the device needed to do was in-dex into a forwarding table using a destination address, and decide where to send the packet next. Over time, forwarding grew more complicated. Middleboxes (e.g., NAT and firewalls) and encapsulation mechanisms (e.g., NAT and firewalls) and encapsulation firewalls and fir the same physical network. HIPAA [20] rules requi

> FORWARD NETWORKS

Static reachability for IP networks

Software-defined networks

1996

2010



2020

Status Quo

Network Working Group Request for Comments: 2418 Obsoletes: 1603 BCP: 25 Category: Best Current Practice

> IETF Working Group Guidelines and Procedures

"We believe in rough consensus and running code"

Copyright (C) The Internet Society (1998). All Rights Reserved.

Abstract

The Internet Engineering Task Force (IETF) has responsibility for developing and reviewing specifications intended as Internet Standards. IETF activities are organized into working groups (WGs). This document describes the guidelines and procedures for formation and operation of IETF working groups. It also describes the formal relationship between IETF participants WG and the Internet Engineering Steering Group (IESG) and the basic duties of IETF participants, including WG Chairs, WG participants, and IETF Area Directors

S. Bradner Editor Harvard University September 1998

Shaky Foundations



"The system doesn't have a semantics; in a very deep sense the program does not have a meaning; what it has is... it's just whatever happens. That's kind of the way nature works too, right?"

Bill Joy

Language-Based Approach



FPGAs + **Smart NICs** **Programmable Fixed-Function** ASICs

ASICs

Software **Switches**

Anatomy of a P4 Program

```
// Programmer-defined types
S
        header hop {
U
          bit<7> port;
          bit<1> bos;
        struct headers {
          hop[9] hops;
        // Programmer-defined components
        parser MyParse(packet_in pkt,
                       out headers hdrs,
inout std_meta met
U
          state start {
            pkt.extract(hdrs.hops.next);
            transition select(hdrs.hops.]
              1: accept;
Π
              default: start;
        control MyPipe(inout headers hdrs
                       inout std_meta met
          action allow() { }
          action deny() { meta.egress_por
          table acl {
            key = { meta.ingress_port :
                    meta.egress_port : ex
S
            actions = { allow; deny; }
            default_action = deny();
ontro
          apply {
            meta.egress_port =
              (bit<8>)hdrs.hops[0].port;
            if(!hdrs.hops[0].isValid()) @
            hdrs.hops.pop_front(1);
            acl.apply();
          }
        control MyDeparse(packet_out pkt
                          in headers hdrs
          apply { pkt.emit(hdrs.hops); }
        Switch(MyParse(),MyPipe(),MyDepar
```

S

ta) {
last.bos) {
-
s, ta) {
rt = 0xFF; }
exact; xact; }
exit;
s) {
<pre>rse()) main;</pre>

Formalization Challenges

The "official" definition of P4 resides in an informal specification and a 40KLoC C++ implementation

P4₁₆ Language Specification

version 1.2.1

The P4 Language Consortium

2020-06-11

Abstract. P4 is a language for programming the data plane of network devices. This document provides a precise definition of the P416 language, which is the 2016 revision of the P4 language (http://p4.org). The target audience for this document includes developers who want to write compilers, simulators, IDEs, and debuggers for P4 programs. This document may also be of interest to P4 programmers who are interested in understanding the syntax and semantics of the language at a deeper level.

Contents

- 1. Scope
- 2. Terms, definitions, and symbols
- 3. Overview
 - 3.1. Benefits of P4
 - 3.2. P4 language evolution: comparison to previous versions (P4 v1.0/v1.1)
- 4. Architecture Model
 - 4.1. Standard architectures
 - 4.2. Data plane interfaces
 - 4.3. Extern objects and functions

5. Example: A very simple switch

5.1 Vary Simple Switch Architecture

Formalization Challenges

The "official" definition of P4 resides in an informal specification and a 40KLoC C++ implementation



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Pull requests Issues Marketplace	e Explore	오 + - 🚳 -	
⊙ U	nwatch 👻 74 ਵਿੱ	े Star 275 रिंग 216	
Dell requests 25 Delto Actions 🛄 Proje	ects 1 🛛 🖽 Wiki	Security	
⊙ 0 tags Go to file Add file -	⊻ Code -	About ණ	
ss; two mor 🚥 🗸 c090794 22 hours ago 🕚) 2,133 commits	P4_16 reference compiler	
d Bazel build files for p4c (#2430)	3 months ago	本 Apache-2.0 License	
EBPF parenthesis issue (#2570)	4 days ago		
date p4_library Bazel rule to allow workspace-r29 days agoReleasese /usr/bin/env bash instead of /bin/bash (#2285)6 months agoNo releases published			
move format prefix from ::error; fixes #2197 (#	8 months ago	Packages	
association pass; two more strength-reduction	22 hours ago	No packages published	
bugs related to StructureExpressions (#2552)	3 days ago	Publish your first package	

Challenge: Undefined Values

8.22. Reading uninitialized values and writing fields of invalid headers

As mentioned in Section 8.17, any reference to an element of a header stack hs[index] where index is a compile-time constant expression must give an error at compile time if the value of the index is out of range. That section also defines the run time behavior of the expressions hs.next and hs.last, and the behaviors specified there take precedence over anything in this section for those expressions.

All mentions of header stack elements in this section only apply for expressions hs[index] where index is a run time variable expression, i.e. not a compile-time constant value. A P4 implementation is allowed not to support hs[index] where index is a run time variable expression, but if it does support these expressions, the implementation should conform to the behaviors specified in this section.

The result of reading a value in any of the situations below is that some unspecified value will be used for that field.

- reading a field from a header that is currently invalid.
- since the header was last made valid.
- **control** or **action** (this list of examples is not intended to be exhaustive).
- range for the header stack.

• reading a field from a header that is currently valid, but the field has not been initialized

• reading any other value that has not been initialized, e.g. a field from a struct, any uninitialized variable inside of an action or control, or an out parameter of a control or action you have called, which was not assigned a value during the execution of that • reading a field of a header that is an element of a header stack, where the index is out of

p4c: Unsound Optimization



fruffy commented on Apr 17 • edited +

Hello.

I have another clarification question on This issue is quite esoteric but has given

```
control ingress(inout Headers h, inour
apply {
    h.h.setInvalid();
    h.h.a = 1;
    h.eth_hdr.src_addr = h.h.a;
    if (h.eth_hdr.src_addr != 1) {
        h.h.setValid();
        h.h.a = 1;
    }
}
```

which is eventually turned into

```
control ingress(inout Headers h, inou
apply {
    h.h.setInvalid();
    h.h.a = 48w1;
    h.eth_hdr.src_addr = 48w1;
  }
}
```

	Contributor 😳 …			
setInvalid , this is a follow-up to #2212. In me some trouble recently.				
t Meta m, inout standard_mo	etadata_t sm) {			
{				
t Meta m, inout standard_me	etadata_t sm) {			

Petr4 Architecture



Petr4 Architecture



Petr4 Architecture



Modular design allows customizing semantics for each architecture

Ту	pes		
ho ::=	bool	booleans	
	int	integers	
	bit $\langle exp \rangle$	bitstrings	
	error $\{\overline{f}\}$	errors	
	match_kind $\{\overline{f}\}$	match kinds	5
	enum $X \{\overline{f}\}$	enums	
	$\{\overline{f:\tau}\}$	records	
	header $\{\overline{f:\tau}\}$	headers	
İ	$\tau[n]$	stacks	
	X	type variabl	es
au ::=	ρ		data types
	table		tables
İ	function $\langle \overline{X} \rangle (\overline{d x})$	$\overline{(:\rho)} \rightarrow \rho_{ret}$	functions
İ	$\operatorname{ctor}(\overline{x:\tau}) \to \tau_{re}$	t	constructors
d ::=	in		copy-in
	out		copy-out
İ	inout		copy-in-out

Petr4 Syntax

Expressions

exp ::= b n_w $\boldsymbol{\mathcal{X}}$ $exp_1[exp_2]$ $exp_1[exp_2:exp_3]$ $\ominus exp$ $exp_1 \oplus exp_2$ $(\tau) exp$ $\{\overline{f = exp}\}$ exp.f X.f $exp\langle\overline{\rho}\rangle(\overline{exp})$

booleans integers variables array accesses bitstring slices unary ops binary ops casts records fields type members function call

Statements

method call stmt $::= exp\langle \overline{\rho} \rangle (\overline{exp})$ assignment $exp \coloneqq exp$ if (exp) stmt else stmt conditional $\{\overline{stmt}\}$ sequencing exit exit return *exp* return var_decl variable declaration

Petr4 Semantics

Type System

 $\Sigma, \Gamma, \Delta \vdash exp : funct$ $\Sigma, \Delta[\overline{X = \rho}] \vdash \overline{\tau} \rightsquigarrow \overline{\tau'} \qquad \Sigma, \Gamma, \Delta \vdash exp \langle \overline{\rho} \rangle$ $\Sigma, \Gamma, \Delta \vdash exp \langle \overline{\rho} \rangle$

Operational Semantics

 $\langle C, \Delta, \sigma, \epsilon, exp \rangle \Downarrow \langle \sigma_1, clos \rangle \langle \Delta[\overline{X = \rho}], \\ \langle C, \Delta, \sigma_1, \epsilon, \overline{d \ x} : \tau' := exp \rangle \\ \langle C, \Delta[\overline{X = \rho}], \sigma_2, \epsilon_c[\overline{x \mapsto \ell}], \\ \langle C, \Delta_2, \sigma_3, \epsilon_2, stmt \rangle \Downarrow \langle \sigma_4, \epsilon_3, return \ val \rangle \\ \langle C, \Delta, \sigma, \sigma, \epsilon_2, stmt \rangle = \langle C, \Delta, \sigma, \sigma, \epsilon_2, stmt \rangle \rangle$

 $\langle C, \Delta, \sigma, \epsilon, exp\langle \overline{\rho} \rangle$

$$\frac{\operatorname{tion}\langle \overline{X}\rangle(\overline{d\ x}:\tau) \to \tau_{ret}}{p:\tau' \operatorname{goes} d} \xrightarrow{\Sigma, \Delta[\overline{X}=\rho]} \vdash \tau_{ret} \rightsquigarrow \tau'_{ret}}_{\Gamma-CALL}$$

$$\frac{\overline{\langle exp\rangle}:\tau'_{ret} \operatorname{goes} \operatorname{in}}{\Gamma-CALL}$$

$$\begin{aligned} s(\epsilon_{c}, \overline{X}, \overline{d \ x} : \tau, \tau, \overline{decl} \ stmt) \rangle \\ \sigma, \epsilon, \overline{\tau} \rangle \Downarrow_{\tau} \overline{\tau'} \\ \gamma \underset{decl}{\Downarrow} \langle \sigma_{2}, \overline{x} \mapsto \ell, \overline{lval} := \ell \rangle \\ \overline{decl} \Downarrow \langle \Delta_{2}, \sigma_{3}, \epsilon_{2}, \text{continue} \rangle \\ \gamma \underset{decl}{\forall} \langle C, \Delta, \sigma_{4}, \epsilon, \overline{lval} := \sigma_{4}(\ell) \rangle \Downarrow_{write} \sigma_{5} \\ \gamma \underset{(\overline{exp})}{(\overline{exp})} \Downarrow \langle \sigma_{5}, val \rangle \end{aligned}$$
E-CALL

Petr4 Metatheory

and (iii) $\Sigma, \Gamma, \Delta \vdash stmt \dashv \Sigma', \Gamma'$.

THEOREM 3.2. Let $\langle C, \Delta, \sigma, \epsilon, stmt \rangle$ be an initial configuration and take contexts $\Xi, \Sigma, \Gamma, \Delta$. Suppose the configuration is safe under the contexts with typing outputs Σ' and Γ' and $\Sigma \vdash \langle \sigma, \epsilon \rangle$. There exists a final configuration $\langle \sigma', \epsilon', sig \rangle$ and a store typing $\Xi' \supseteq \Xi$ such that $\langle C, \Delta, \sigma, \epsilon, stmt \rangle \Downarrow \langle \sigma', \epsilon', sig \rangle$ and $\Xi', \Sigma', \Gamma', \Delta \vdash \langle \sigma', \epsilon', sig \rangle$.

Proof is mostly standard, but needs a

Definition 3.1. A statement configuration $\langle C, \Delta, \sigma, \epsilon, stmt \rangle$ is said to be safe under $\Xi, \Sigma, \Gamma, \Delta$ with typing outputs Σ', Γ' , written $\Xi, \Sigma, \Gamma, \Delta \vdash \langle C, \Delta, \sigma, \epsilon, stmt \rangle \dashv \Sigma', \Gamma'$, if (i) $\Xi, \Delta \vdash \sigma$, (ii) $\Xi, \Delta \vdash \epsilon \colon \Gamma$,

logical relations argument for termination...

Future Work

 Poulet4: Coq port (with Princeton gang) Verified compiler transformations -Inlining functions / controls -Parser unrolling / vectorization -Code motion Code generation for new targets -eBPF -FPGAs -Bluespec/Kami/ChiselFlow





- Final Project (due today; 48-hour extension until Friday)
- Course Evaluations!
- (Regrades)





Cornell Courses

- CS 4120 (Compilers)
- CS 5114 / 6114 (Network PL)
- CS 6110 (Advanced PL)
- CS 6120 (Advanced Compilers)
- CS 61xx (Special Topics)

Research

- CS 4999
- Summer
- Open Source (e.g., GSOC)

After 4110



Doing a PhD...

Applications

- Transcript
- Recommendation Letters
- Statements
- (GRE)

Masters Degree?

• Optional not required (in North America)

Conferences

- SIGPLAN "Big 4": POPL, PLDI, ICFP, OOPSLA
- Programming Languages Mentoring Workshop (PLMW)

Compilers

- GPUs
- TPUs
- LLVM
- WebAssembly
- Rust

Verification

- Startups (Bedrock Systems, Correct Computation, etc.)
- Amazon Automated Reasoning Group
- Google Project Oak

Industry



- CS 4110 is one of my favorite classes to teach...
- Hybrid classes are hard for all of us...
- Thanks for your enthusiasm this semester, for engaging in Zoom, and for patience with my tech SNAFUs
- Please keep in touch!

Thank you!