Finite State Machines

Hakim Weatherspoon
CS 3410
Computer Science
Cornell University

The slides are the product of many rounds of teaching CS 3410 by Professors Weatherspoon, Bala, Bracy, and Sirer.
Stateful Components

Combinational logic

• Output computed directly from inputs
• System has no internal state
• Nothing depends on the past!

Need:

• To record data
• To build stateful circuits
• A state-holding device

Sequential Logic & Finite State Machines
Finite State Machines

An electronic machine which has

- external inputs
- externally visible outputs
- internal state

Output and next state depend on

- inputs
- current state
Abstract Model of FSM

Machine is

\[ M = (S, I, O, \delta) \]

- **S**: Finite set of states
- **I**: Finite set of inputs
- **O**: Finite set of outputs
- **\( \delta \)**: State transition function

Next state depends on present input and present state
Finite State Machine

- inputs from external world
- outputs to external world
- internal state
- combinational logic
Input: **up** or **down**
Output: **on** or **off**
States: **A**, **B**, **C**, or **D**
Input: \( \uparrow = \text{up} \) or \( \downarrow = \text{down} \)
Output: \( \uparrow = \text{on} \) or \( \downarrow = \text{off} \)
States: \( A, B, C, \) or \( D \)
Input: 0 = up or 1 = down
Output: 1 = on or 0 = off
States: 00 = A, 01 = B, 10 = C, or 11 = D
Outputs and next state depend on both current state and input

General Case: Mealy Machine

Mealy Machine
Special Case: Moore Machine

Outputs depend only on current state
Moore Machine FSM Example

Input: up or down
Output: on or off
States: A, B, C, or D
Input: **up** or **down**
Output: **on** or **off**
States: **A**, **B**, **C**, or **D**
Add two infinite input bit streams

- streams are sent with least-significant-bit (lsb) first

...10110

...01111

Sum: output

...00101

...01111
Add two infinite input bit streams

- streams are sent with least-significant-bit (lsb) first

```
...10110
...01111
```

**Carry-out**

1

```
...00101
```

**Sum: output**
Add two infinite input bit streams

- streams are sent with least-significant-bit (lsb) first

```
...10110

...01111
```

Carry-in

Sum: output

```
...00101
```
Add two infinite input bit streams

- streams are sent with least-significant-bit (lsb) first

Carry-\textit{out}:

\[ \ldots 10110 \rightarrow \ldots 00101 \]

Sum: output

\[ \ldots 01111 \rightarrow \ldots 00101 \]
Add two infinite input bit streams

- streams are sent with least-significant-bit (lsb) first

How many states are needed to represent FSM

a) 0
b) 1
c) 2
d) 3
e) 4
Strategy for Building an FSM

(1) Draw a state diagram (e.g. Mealy Machine)
(2) Write output and next-state tables
(3) Encode states, inputs, and outputs as bits
(4) Determine logic equations for next state and outputs
(5) Draw the Circuit
FSM: State Diagram

2 states ___ and ___
Inputs: ___ and ___
Output: ____
Two states: S0 (no carry in), S1 (carry in)

Inputs: a and b

Output: z

- z is the sum of inputs a, b, and carry-in (one bit at a time)
- A carry-out is the next carry-in state.
Two states: $S_0$ (no carry in), $S_1$ (carry in)

Inputs: $a$ and $b$

Output: $z$

- $z$ is the sum of inputs $a$, $b$, and carry-in (one bit at a time)
- A carry-out is the next carry-in state.
- Arcs labeled with input bits $a$ and $b$, and output $z$
Two states: S0 (no carry in), S1 (carry in)

Inputs: a and b

Output: z

- z is the sum of inputs a, b, and carry-in (one bit at a time)
- A carry-out is the next carry-in state.
- Arcs labeled with input bits a and b, and output z (Mealy Machine)
Is this a Moore or Mealy Machine?

a) Moore

b) Mealy

c) Cannot be determined
Is this a Moore or Mealy Machine?

a) Moore

b) Mealy

c) Cannot be determined
(2) Write down all input and state combinations
(2) Write down all input and state combinations

<table>
<thead>
<tr>
<th>a</th>
<th>b</th>
<th>Current state</th>
<th>z</th>
<th>Next state</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>S0</td>
<td>0</td>
<td>S0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>S0</td>
<td>1</td>
<td>S0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>S0</td>
<td>1</td>
<td>S0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>S0</td>
<td>0</td>
<td>S1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>S1</td>
<td>1</td>
<td>S0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>S1</td>
<td>0</td>
<td>S1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>S1</td>
<td>0</td>
<td>S1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>S1</td>
<td>1</td>
<td>S1</td>
</tr>
</tbody>
</table>
(3) Encode states, inputs, and outputs as bits

Two states, so 1-bit is sufficient

- A single flip-flop will encode the state
(4) Determine logic equations for next state and outputs

Combinational Logic Equations

\[ z = \overline{ab}s + \overline{a}bs + \overline{ab}s + abs \]

\[ s' = ab\overline{s} + \overline{a}bs + a\overline{b}s + abs \]
(4) Determine logic equations for next state and outputs

Combinational Logic Equations

\[ z = \overline{a}b\overline{s} + a \overline{b}s + \overline{a}bs + abs \]

\[ s' = ab\overline{s} + \overline{a}bs + a\overline{b}s + abs \]
Sequential Logic Circuits

Strategy:
(1) Draw a state diagram (e.g. Mealy Machine)
(2) Write output and next-state tables
(3) Encode states, inputs, and outputs as bits
(4) Determine logic equations for next state and outputs

Next State $s'$

Current State $s$

Input $a, b$

D Q

Next State $s' = ab\bar{s} + \bar{a}bs + a\bar{b}s + abs$

Output $z$

Comb. Logic

$z = \bar{a}bs + a\bar{b}s + \bar{a}bs + abs$
Which statement(s) is true

(A) In a Moore Machine output depends on both current state and input
(B) In a Mealy Machine output depends on both current state and input
(C) In a Mealy Machine output depends on next state and input
(D) All the above are true
(E) None are true
Which statement(s) is true

(A) In a Moore Machine output depends on both current state and input

(B) In a Mealy Machine output depends on both current state and input

(C) In a Mealy Machine output depends on next state and input

(D) All the above are true

(E) None are true
General Case: Mealy Machine

Outputs and next state depend on both current state and input
Moore Machine

Special Case: Moore Machine

Outputs depend only on current state

Moore Machine Diagram:
- Registers
- Current State
- Input
- Comb. Logic
- Output
- Next State
Example: Digital Door Lock

Digital Door Lock

Inputs:
- keycodes from keypad
- clock

Outputs:
- “unlock” signal
- display how many keys pressed so far
Door Lock: Inputs
Assumptions:

- signals are synchronized to clock
- Password is B-A-B

<table>
<thead>
<tr>
<th>K</th>
<th>A</th>
<th>B</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Ø (no key)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>‘A’ pressed</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>‘B’ pressed</td>
</tr>
</tbody>
</table>
Assumptions:
- High pulse on U unlocks door

Strategy:
1. Draw a state diagram (e.g. Moore Machine)
2. Write output and next-state tables
3. Encode states, inputs, and outputs as bits
4. Determine logic equations for next state and outputs
Door Lock: Simplified State Diagram

(1) Draw a state diagram (e.g. Moore Machine)
Door Lock: Simplified State Diagram

(1) Draw a state diagram (e.g. Moore Machine)
Door Lock: Simplified State Diagram

(2) Write output and next-state tables
(2) Write output and next-state tables
Door Lock: Simplified State Diagram

(2) Write output and next-state tables
Door Lock: Simplified State Diagram

(2) Write output and next-state tables
State Table Encoding

<table>
<thead>
<tr>
<th>S₂</th>
<th>S₁</th>
<th>S₀</th>
<th>D₃</th>
<th>D₂</th>
<th>D₁</th>
<th>D₀</th>
<th>U</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>S₂</th>
<th>S₁</th>
<th>S₀</th>
<th>S'₂</th>
<th>S'₁</th>
<th>S'₀</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>State</th>
<th>S₂</th>
<th>S₁</th>
<th>S₀</th>
</tr>
</thead>
<tbody>
<tr>
<td>Idle</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>G1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>G2</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>G3</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>B1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>B2</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>
(4) Determine logic equations for next state and outputs

\[ U = \overline{S_2}S_1S_0 \]

\[ D_0 = \overline{S_2}S_1S_0 + \overline{S_2}S_1S_0 + S_2\overline{S_1}S_0 \]

\[ D_1 = \overline{S_2}S_1S_0 + \overline{S_2}S_1S_0 + \overline{S_2}S_1S_0 \]
Door Lock: Implementation

<table>
<thead>
<tr>
<th>$S_2$</th>
<th>$S_1$</th>
<th>$S_0$</th>
<th>$K$</th>
<th>$A$</th>
<th>$B$</th>
<th>$S'_2$</th>
<th>$S'_1$</th>
<th>$S'_0$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>x</td>
<td>x</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>x</td>
<td>x</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

$S'_0 = ?$

$S'_1 = ?$

$S'_2 = \overline{S_2 S_1 S_0} K A \overline{B} + \overline{S_2 S_1 S_0} K \overline{A} B + S_2 S_1 S_2 K A \overline{B} + \overline{S_2 S_1 S_0} K + S_2 \overline{S_1 S_0} \overline{K A \overline{B}}$
**Strategy:**

1. Draw a state diagram (e.g. Moore Machine)
2. Write output and next-state tables
3. Encode states, inputs, and outputs as bits
4. Determine logic equations for next state and outputs
Door Lock: Implementation

Strategy:
(1) Draw a state diagram (e.g. Moore Machine)
(2) Write output and next-state tables
(3) Encode states, inputs, and outputs as bits
(4) Determine logic equations for next state and outputs
Summary

We can now build interesting devices with sensors

• Using combinational logic

We can also store data values

• Stateful circuit elements (D Flip Flops, Registers, ...)
• State Machines or Ad-Hoc Circuits