CS 3410 Homework 2   NetID_____ Date:_____
Due Tuesday, February 21st, 2012, 11:59pm   Name:_____

Problem 1.

a) Recall that a flip-flop is made of two latches with opposite enable signals so as to be edge-sensitive rather than level-sensitive. Explain why flip-flops are used for storing state rather than using latches directly.

b) More pipeline stages means higher throughput, so it may seem at first that we should design our processors with as many pipeline stages as possible. Give one reason why more pipeline stages will not always improve the speed of the processor.

c) Give another, different reason why more pipeline stages will not always improve the speed of the processor.

Problem 2.

    a) CPI is a weighted average of how many cycles it takes for a single instruction to be executed. However, CPI alone is not a good measure of CPU performance. Explain why.

    b) Consider a 5 stage pipeline MIPS processor with the following critical length: 3 ns, 2 ns, 4 ns, 3 ns, 3.5 ns. Calculate the following:

        a. Latency (of the entire pipeline)

        b. Throughput

        c. CPI. Assume that 20% of the instructions is a jump/branch followed by a pipeline bubble, and everything else takes one cycle.

Problem 3.

Do part (a) of exercise 4.7 (4.7.1 through 4.7.6) on page 415 of the revised 4th edition of the Patterson and Hennessy book.

Problem 4.

Finite State Machines: Pattern Finder

Design a circuit (with a finite state machine) for finding the *each* occurrence of a specific pattern, 10110010 or 10110 in a very long stream of binary numbers.

Specifically, your circuit will process a very long stream of binary numbers, $b_0 b_1 b_2 b_3 \ldots$ You do not know how long the list will be. Your circuit will be given the ith binary number during the ith clock cycle via the input **B**. If you have not seen the pattern yet, then the output **Found** should be 0; otherwise, if $b_{i-7} b_{i-6} b_{i-5} b_{i-4} b_{i-3} b_{i-2} b_{i-1} b_i = 10110010$ or $b_{i-4} b_{i-3} b_{i-2} b_{i-1} b_i = 10110$ then your circuit should set the output **Found** to be 1.

Hint 1: There should be 9 states, one of which is an initial state. If the input pattern were simply the short sequence "10110010," your FSM should reach each state exactly once before the end of the sequence.

Problem 5.

Consider the following C code segment:

int A[10];
x = x + y + z – A[5];

Assume that x, y, and z are stored in registers $s1-$s3, and the base address of array A is stored in register $s0. Note that $t0 is just another register.

   a) Write this code in MIPS assembly.

   b) Write the MIPS assembly instructions you just wrote in 32-bit binary machine code. Separate sets of bits by a single space according to the type of instruction that it is. For example, the function "or $s1, $s2, $s3" is an R-type instruction, and so it would be written
000000 10010 10011 10001 00000 100101

Problems 6.

Suppose we are using the 5-stage pipelined MIPS processor on page 362 of the textbook. This is a processor that does not account for possible pipeline hazards, so it may produce errors on code that does not account for this. The code written below does not account for these hazards. Rewrite the code so that no errors will occur.

All registers contain the value 0 except possibly for $t0, the value of which is unknown.

```
MAIN:
ADDIU $a0, $zero, 10
ADDU $t2, $t0, $a0
ADDIU $t1, $zero, -5
ADDIU $t1, $t1, -1
BNE $t2, $zero, SECTION
ADDIU $t1, $t1, 5

SECTION:
ADDU $v0, $t0, $t2
ADDIU $t0, $t0, 0
ADDIU $t1, $v0, 0
ADDIU $a0, $a0, -1
BNE $a0, $zero, SECTION
ADDIU $t0, $t0, -1234
```

Survey

How long did this homework take you (x hrs)?

How hard did you find this homework (easy/medium/hard)?

Other comments on this homework?