Pipelining

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See: P&H Chapter 4.5
Alice

Bob

They don’t always get along...
The Materials

- Saw
- Drill
- Glue
- Paint
N pieces, each built following same sequence:

- Saw
- Drill
- Glue
- Paint
Alice owns the room
Bob can enter when Alice is finished
Repeat for remaining tasks
No possibility for conflicts
Elapsed Time for Alice: 4
Elapsed Time for Bob: 4
Total elapsed time: 4*N
Can we do better?

Latency:
Throughput:
Concurrency:
Can we do better?
Partition room into *stages of a pipeline*

One person owns a stage at a time
4 stages
4 people working simultaneously
Everyone moves right in lockstep
Pipelined Performance

Latency:

Throughput:

Concurrency:
Unequal Pipeline Stages

Latency:
Throughput:
Concurrency:
Poorly-balanced Pipeline Stages

Latency:
Throughput:
Concurrency:
Latency:
Throughput:
Concurrency:
Splitting Pipeline Stages

Latency:
Throughput:
Concurrency:
Q: What if glue step of task 3 depends on output of task 1?

Latency:  
Throughput:  
Concurrency:
Lessons

Principle:
Latencies can be masked by parallel execution

Pipelining:
• Identify *pipeline stages*
• Isolate stages from each other
• Resolve pipeline *hazards*
A Processor

Instruction Fetch
- Instruction Memory
  - PC
  - New PC

Instruction Decode
- Register File
- ALU
- Immediate (imm)
- Extend

Execute
- Compute Jump/Branch Targets
- New PC += 4

Memory
- Address
- Memory Read

Write-Back
- ALU Write
- Memory Write
Five stage “RISC” load-store architecture

1. Instruction fetch (IF)
   – get instruction from memory, increment PC

2. Instruction Decode (ID)
   – translate opcode into control signals and read registers

3. Execute (EX)
   – perform ALU operation, compute jump/branch targets

4. Memory (MEM)
   – access memory if needed

5. Writeback (WB)
   – update register file
Break instructions across multiple clock cycles (five, in this case)

Design a separate stage for the execution performed during each clock cycle

Add pipeline registers to isolate signals between different stages