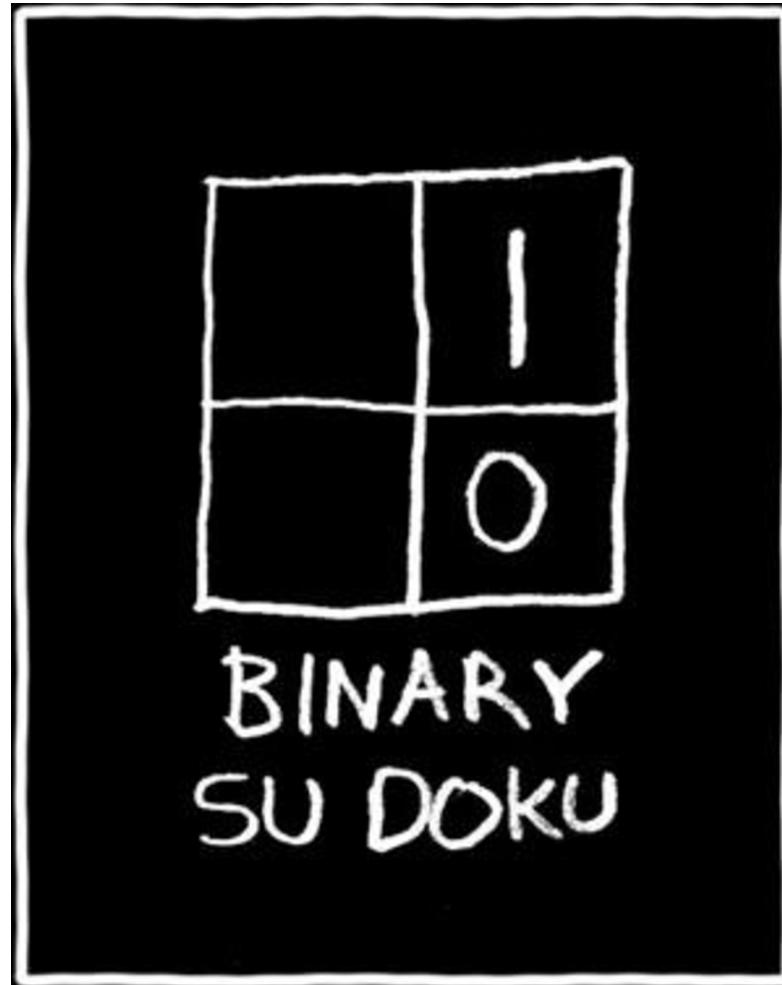
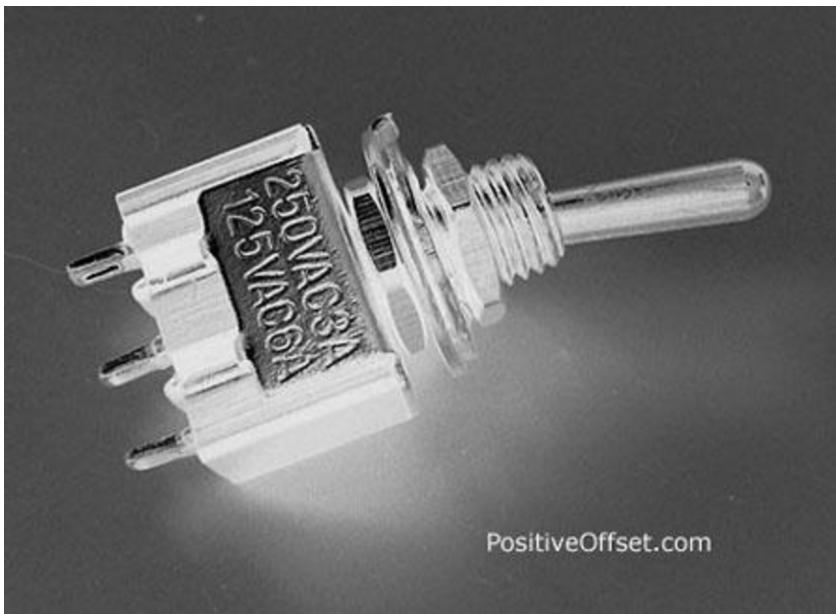


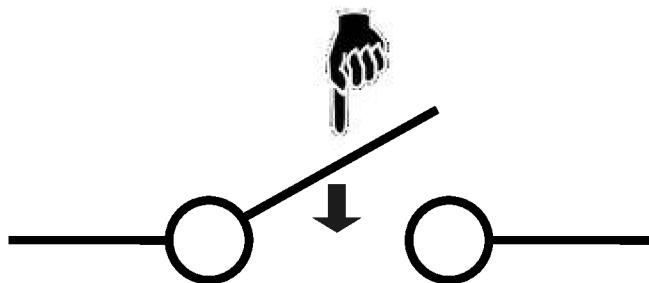
# Gates and Logic



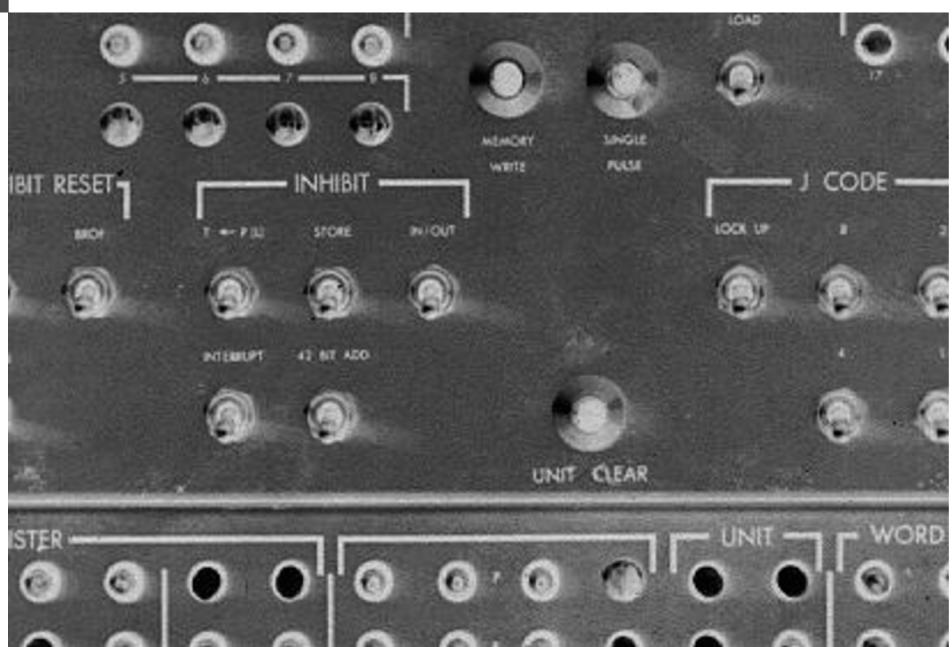
See: P&H Appendix C.2, C.3

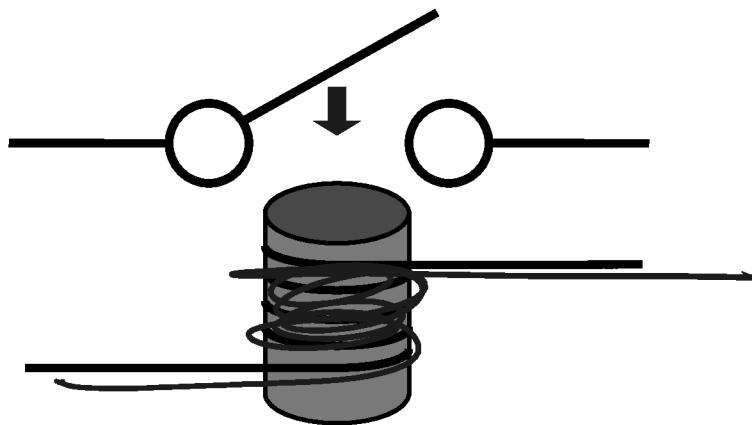


PositiveOffset.com

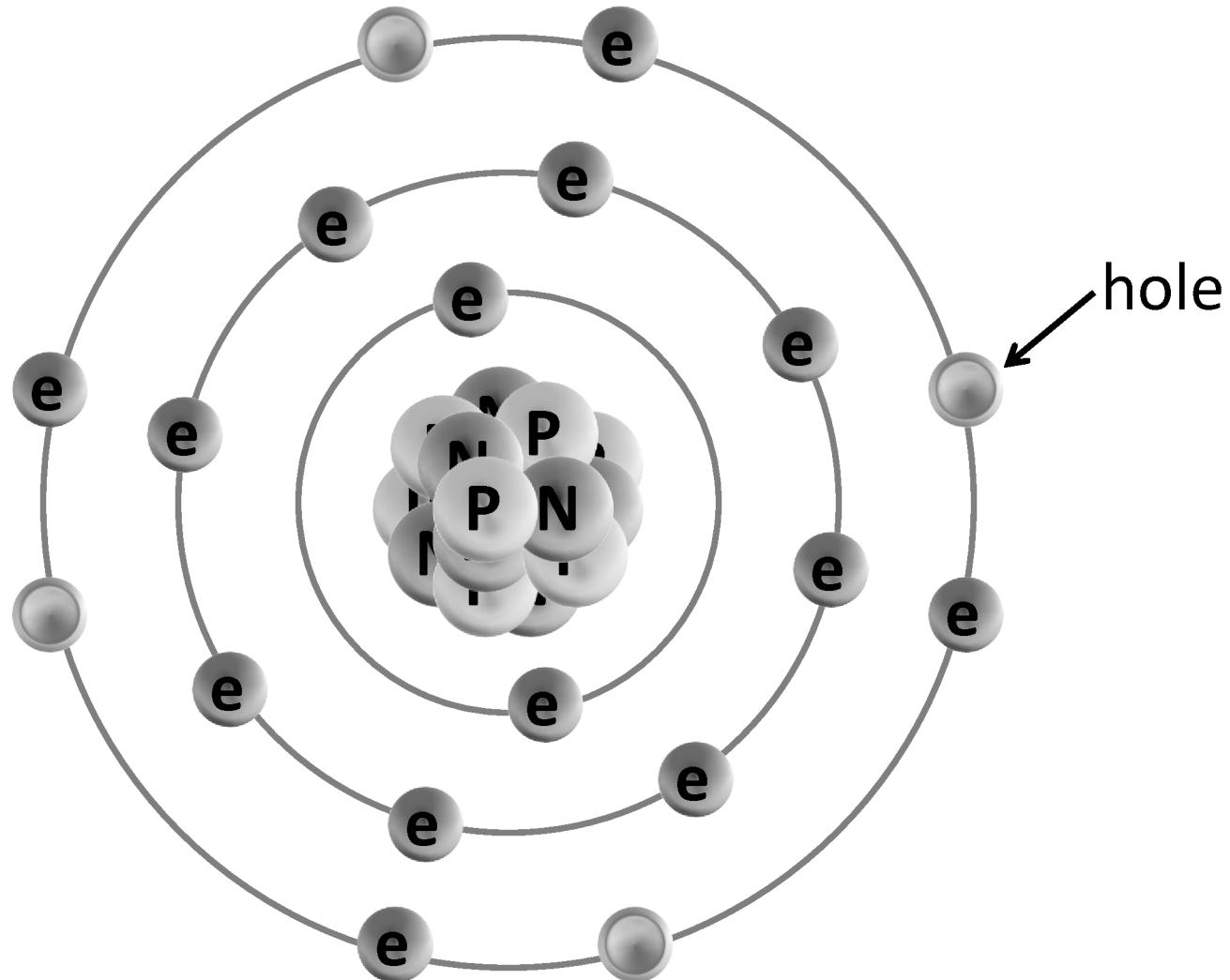


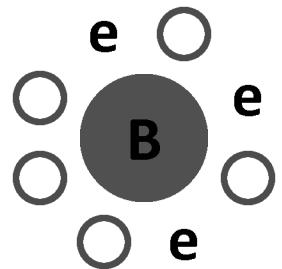
- Acts as a *conductor* or *insulator*
- Can be used to build amazing things...



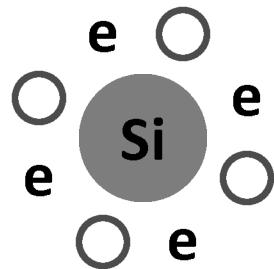


- One current controls another (larger) current
- Static Power:
  - Keeps consuming power when in the *ON* state
- Dynamic Power:
  - Jump in power consumption when switching

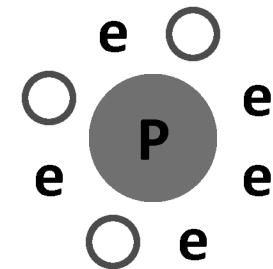




Boron

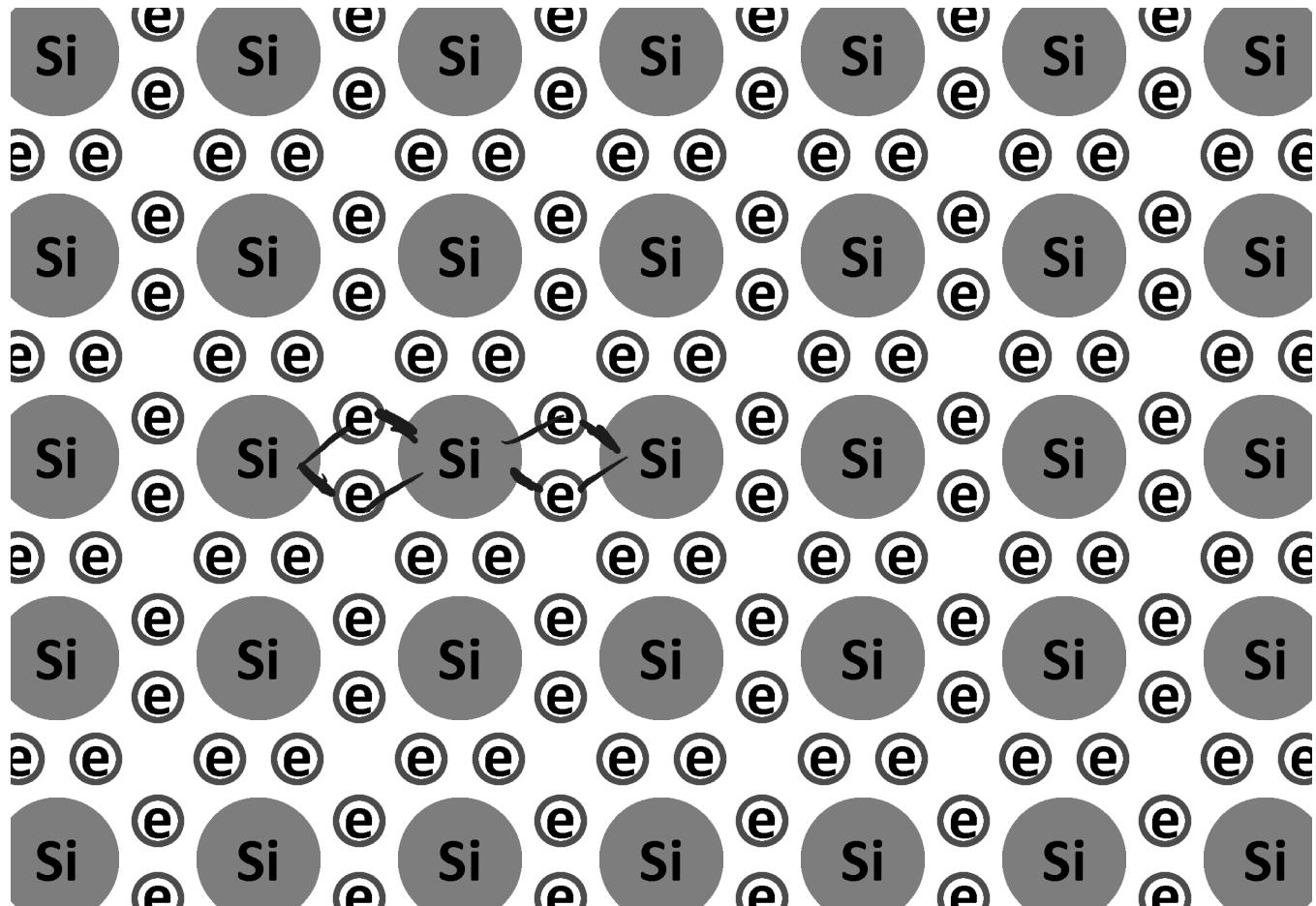


Silicon

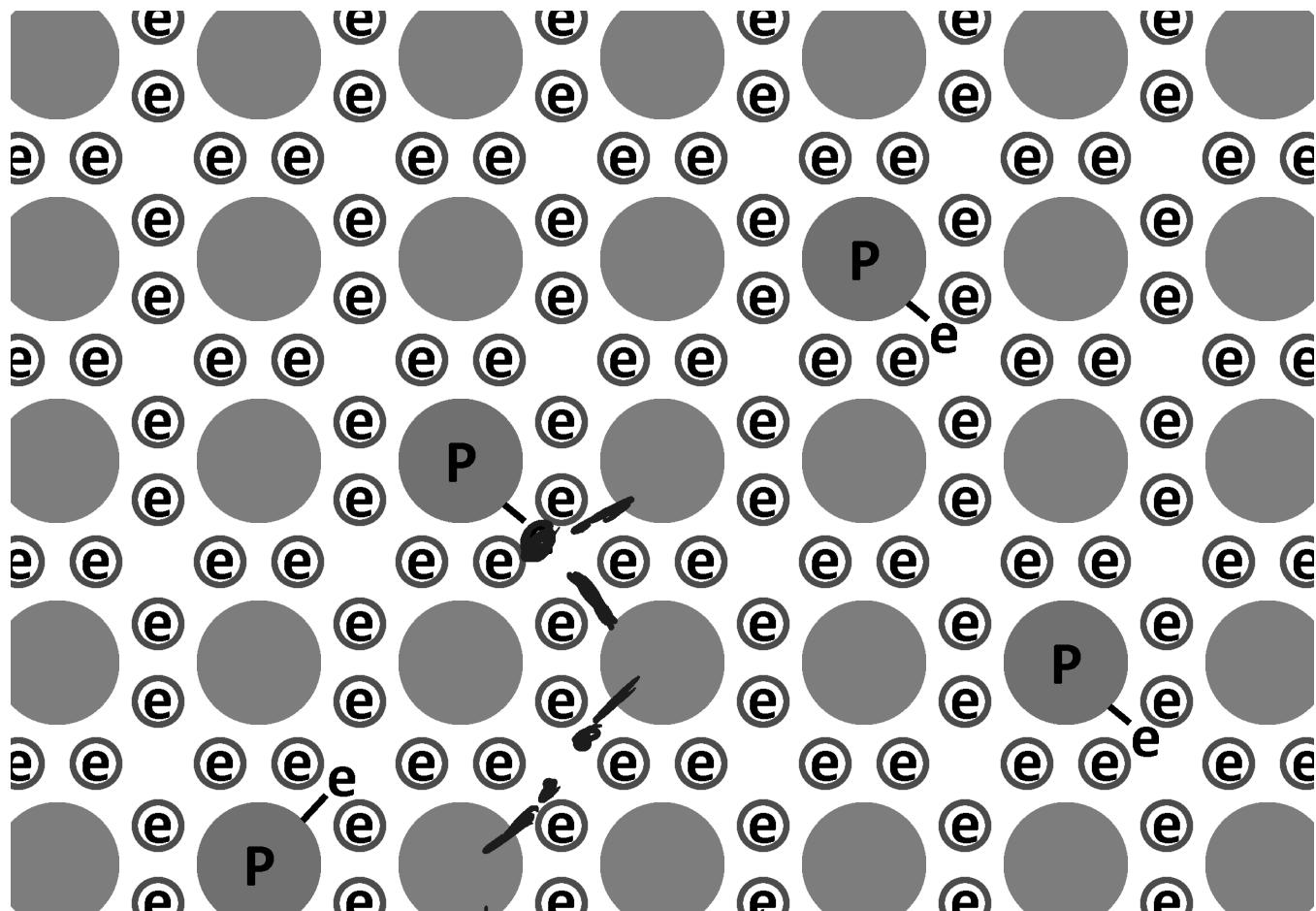


Phosphorus

# Silicon

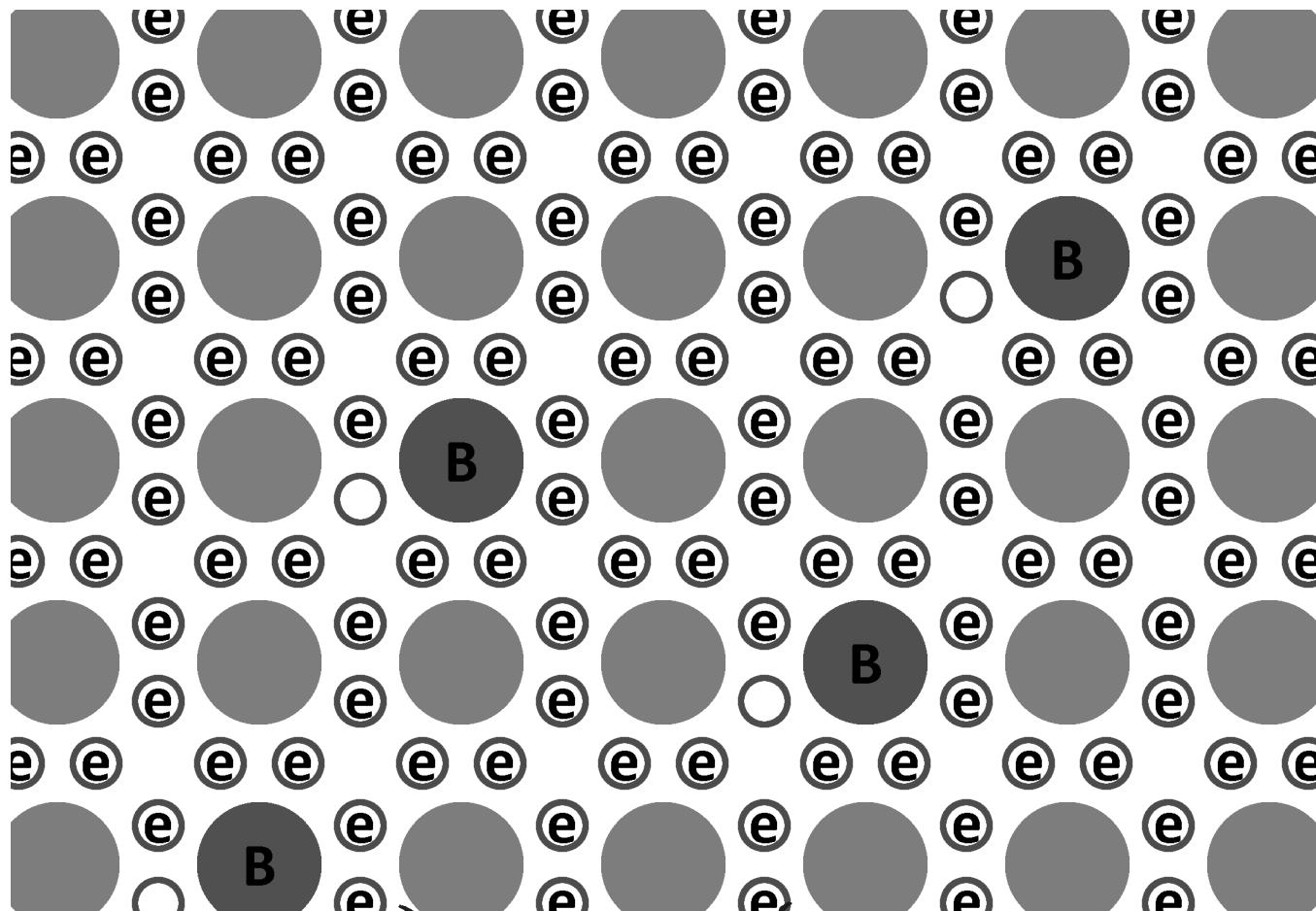


# N-Type: Silicon + Phosphorus



mobile electrons  $\Rightarrow$  conductor  
 $h^- + v^- \rightarrow$  depleted  $\Rightarrow$  ins.

# P-Type: Silicon + Boron



mobile holes  $\Rightarrow$  cond.  
-  $\Rightarrow$  depleted  $\Rightarrow$  ins.



Insulator



p-type (Si+Boron)  
has mobile holes:

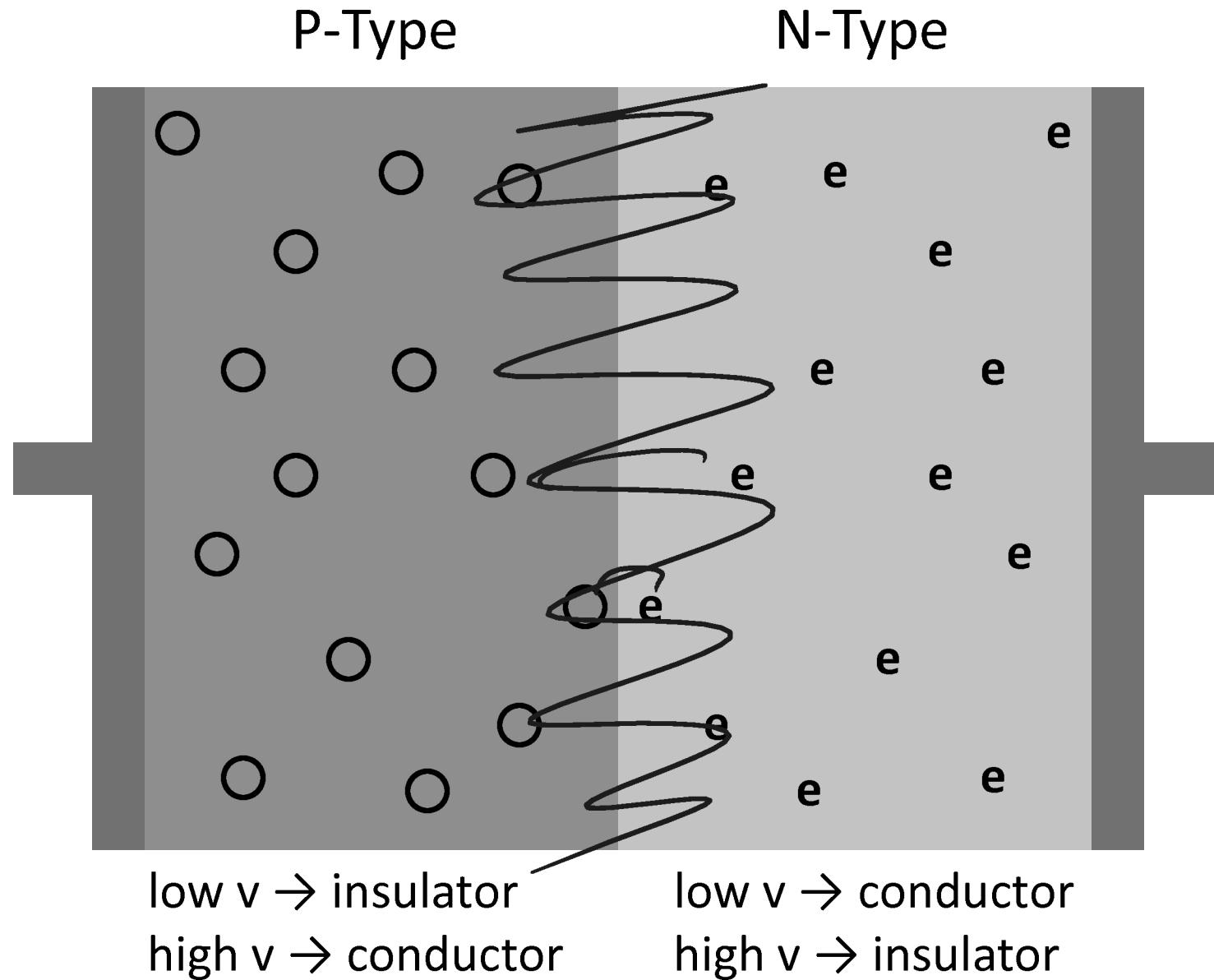
low voltage (depleted)  
→ insulator

high voltage (mobile holes)  
→ conductor

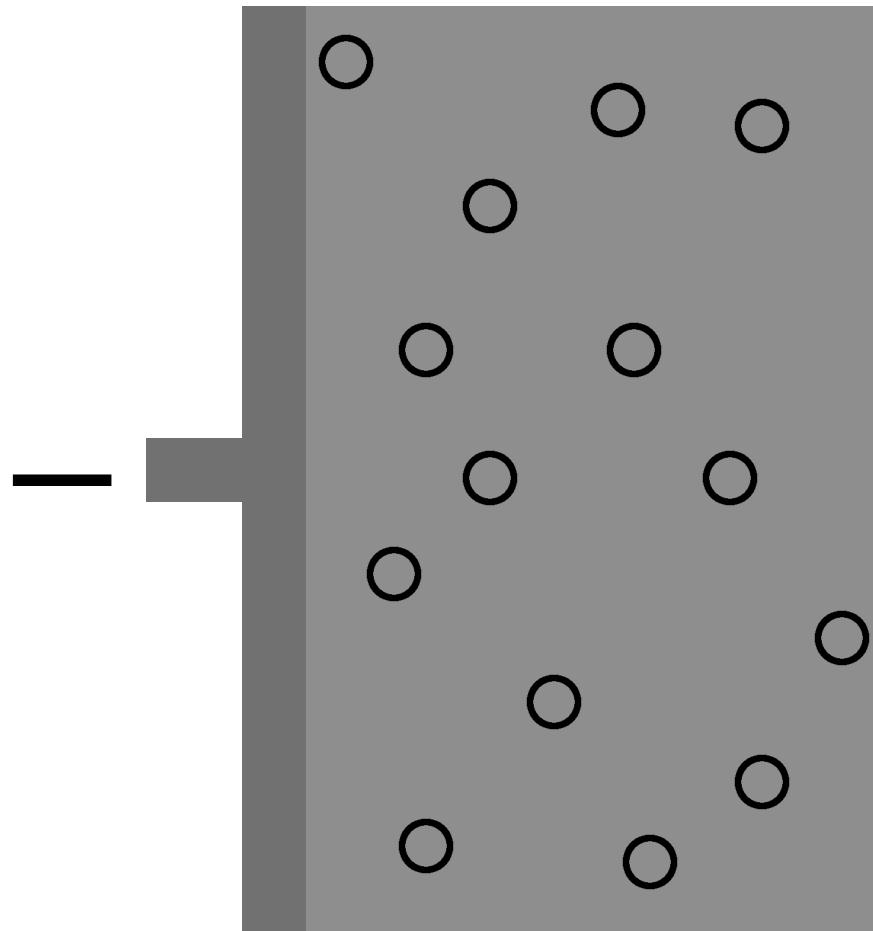
n-type (Si+Phosphorus)  
has mobile electrons:

low voltage (mobile electrons)  
→ conductor

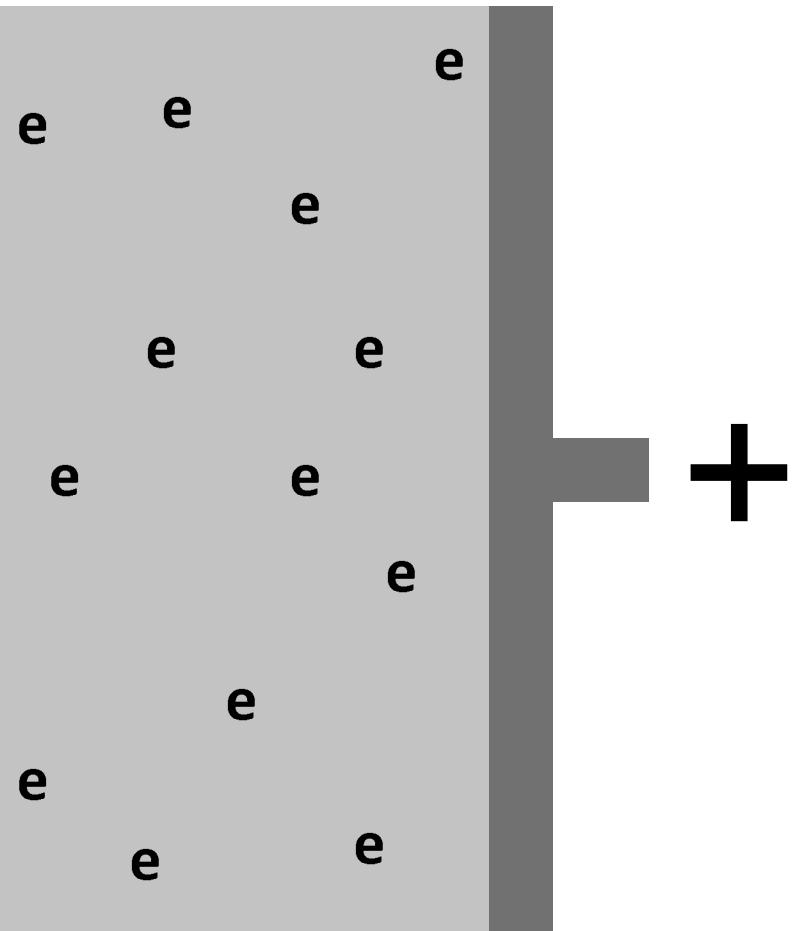
high voltage (depleted)  
→ insulator



P-Type

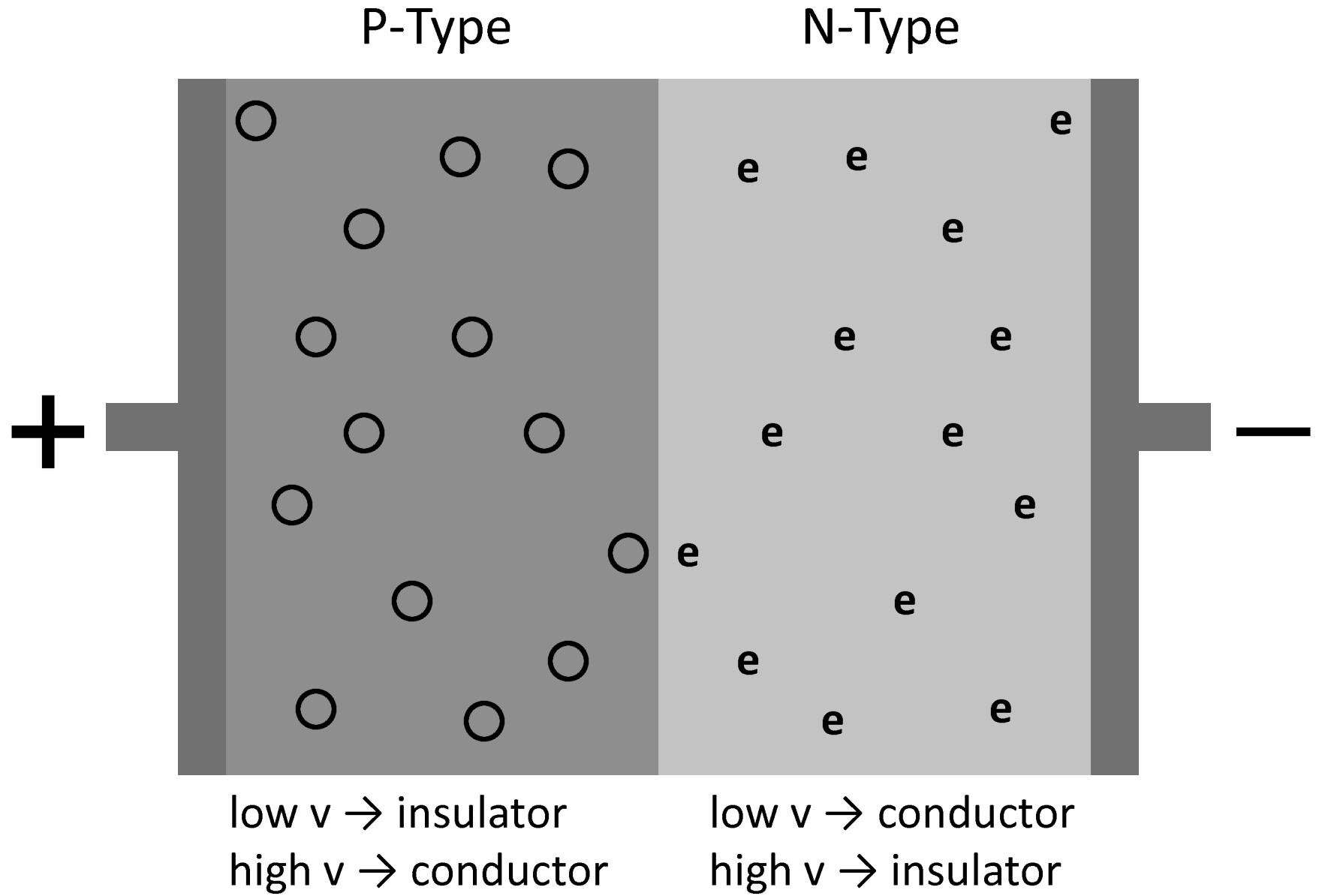


N-Type

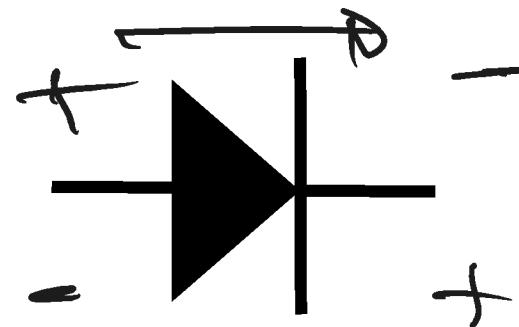
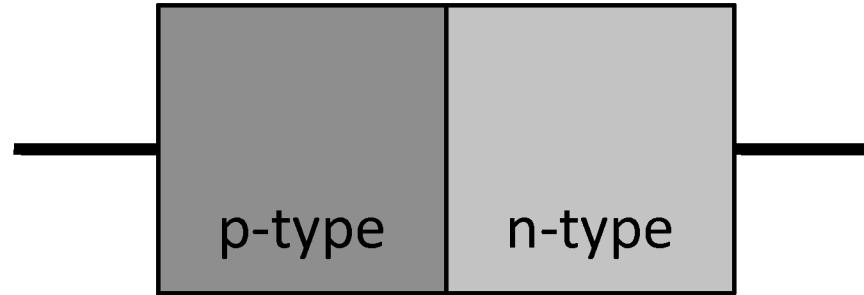
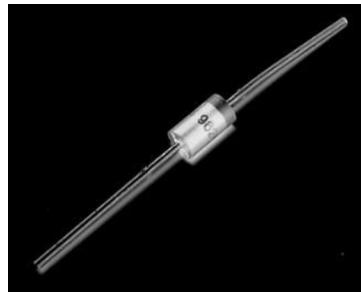


low  $v \rightarrow$  insulator  
high  $v \rightarrow$  conductor

low  $v \rightarrow$  conductor  
high  $v \rightarrow$  insulator



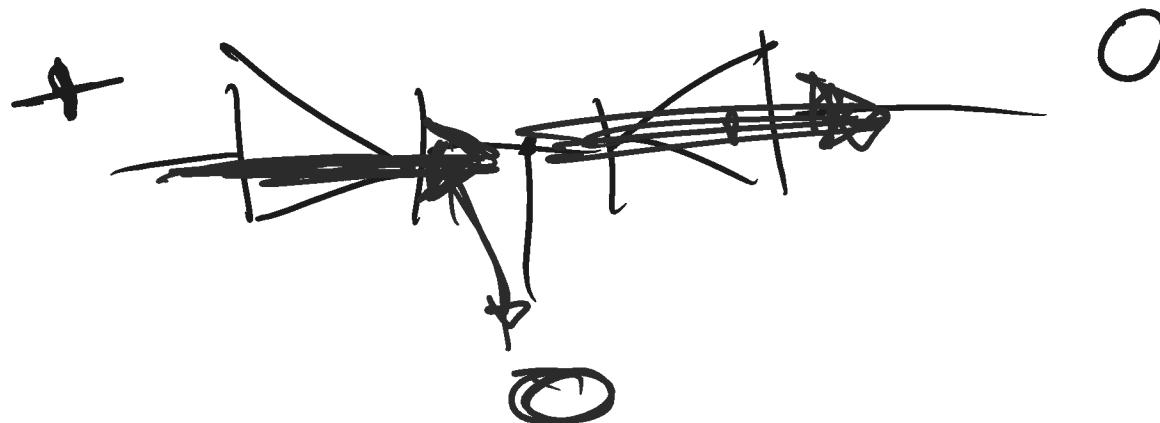
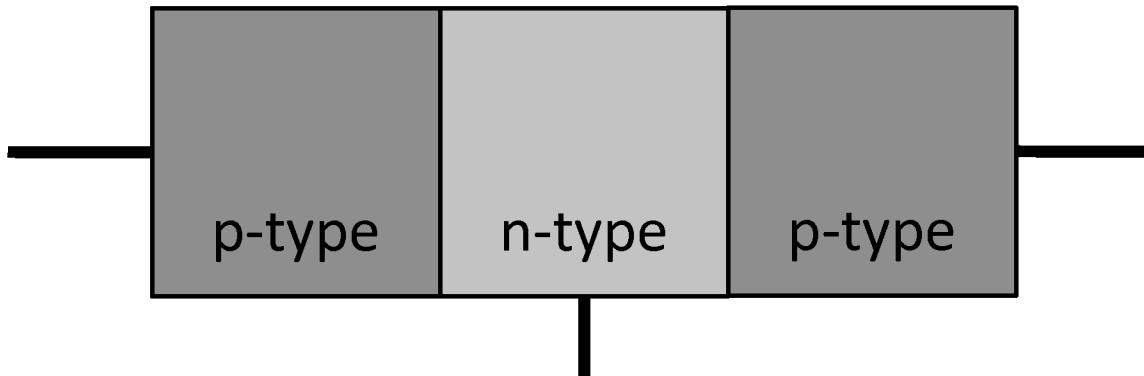
## PN Junction “Diode”

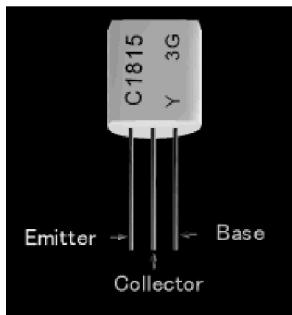


Conventions:

$v_{dd} = v_{cc} = +1.2v = +5v = hi$

$v_{ss} = v_{ee} = 0v = gnd$

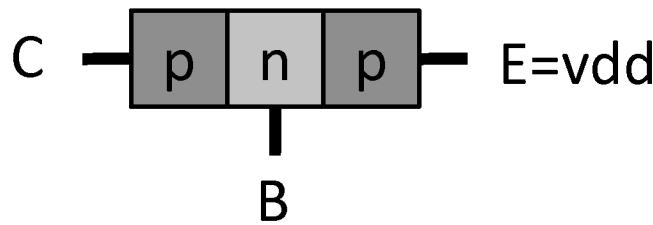




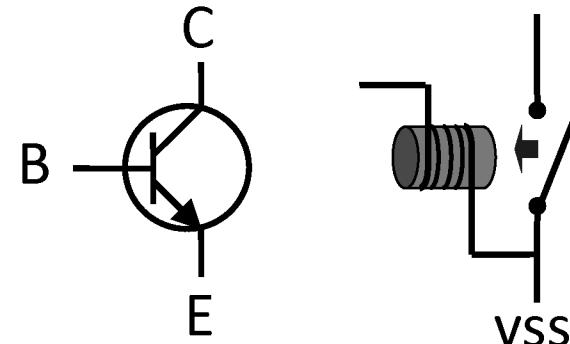
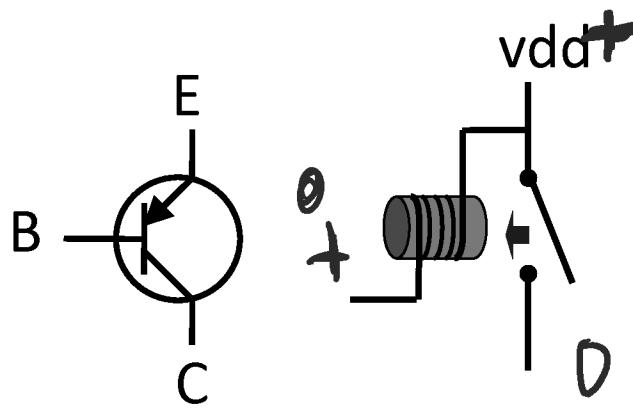
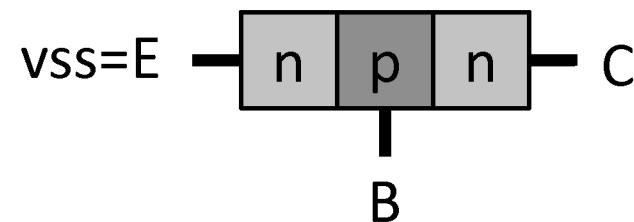
- Solid-state switch: The most amazing invention of the 1900s

Emitter = “input”, Base = “switch”, Collector = “output”

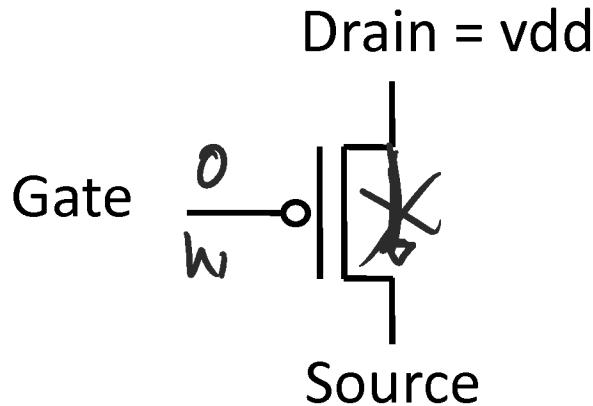
PNP Transistor



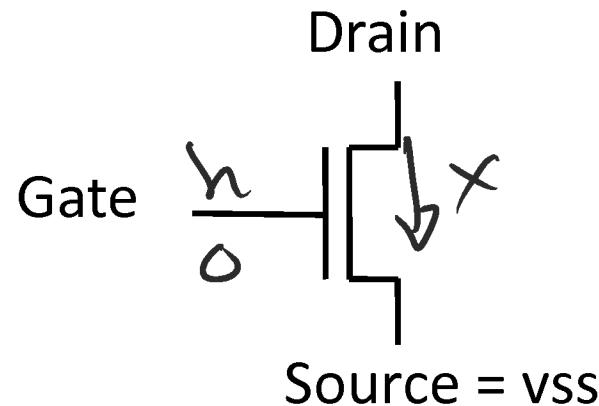
NPN Transistor



## P-type FET

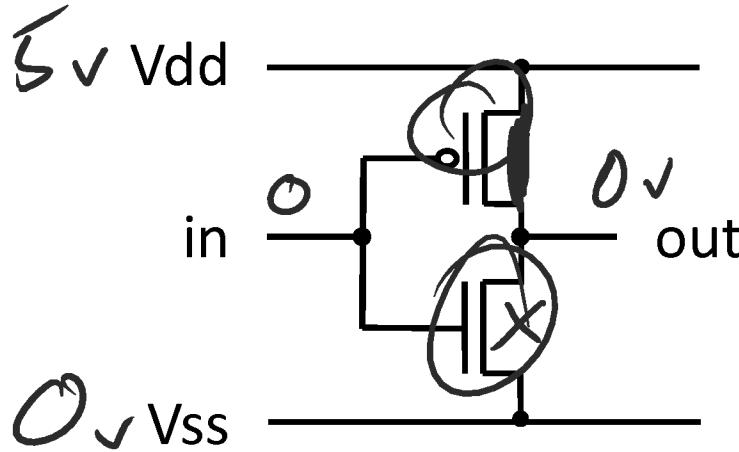


## N-type FET



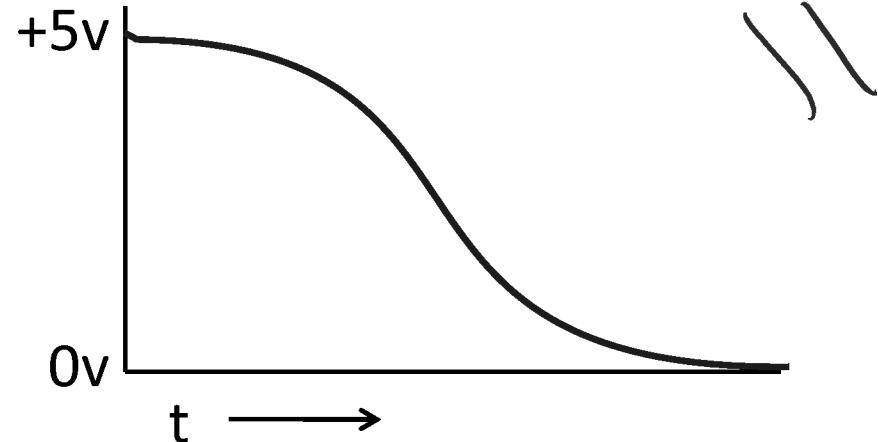
- Connect Source to Drain when Gate = lo
- Drain must be vdd, or connected to source of another P-type transistor

- Connect Source to Drain when Gate = hi
- Source must be vss, or connected to drain of another N-type transistor



In	Out
$5V$	$0V$
$0V$	$5V$

voltage



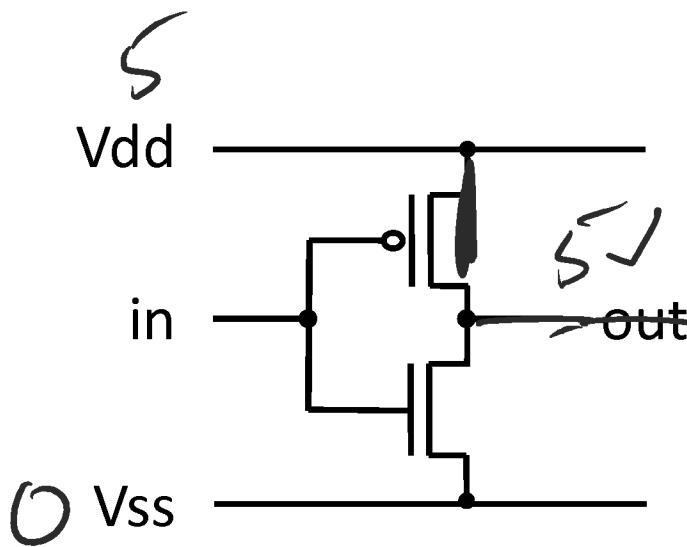
## Gate delay

- transistor switching time
- voltage, propagation, fanout, temperature, ...

## CMOS design

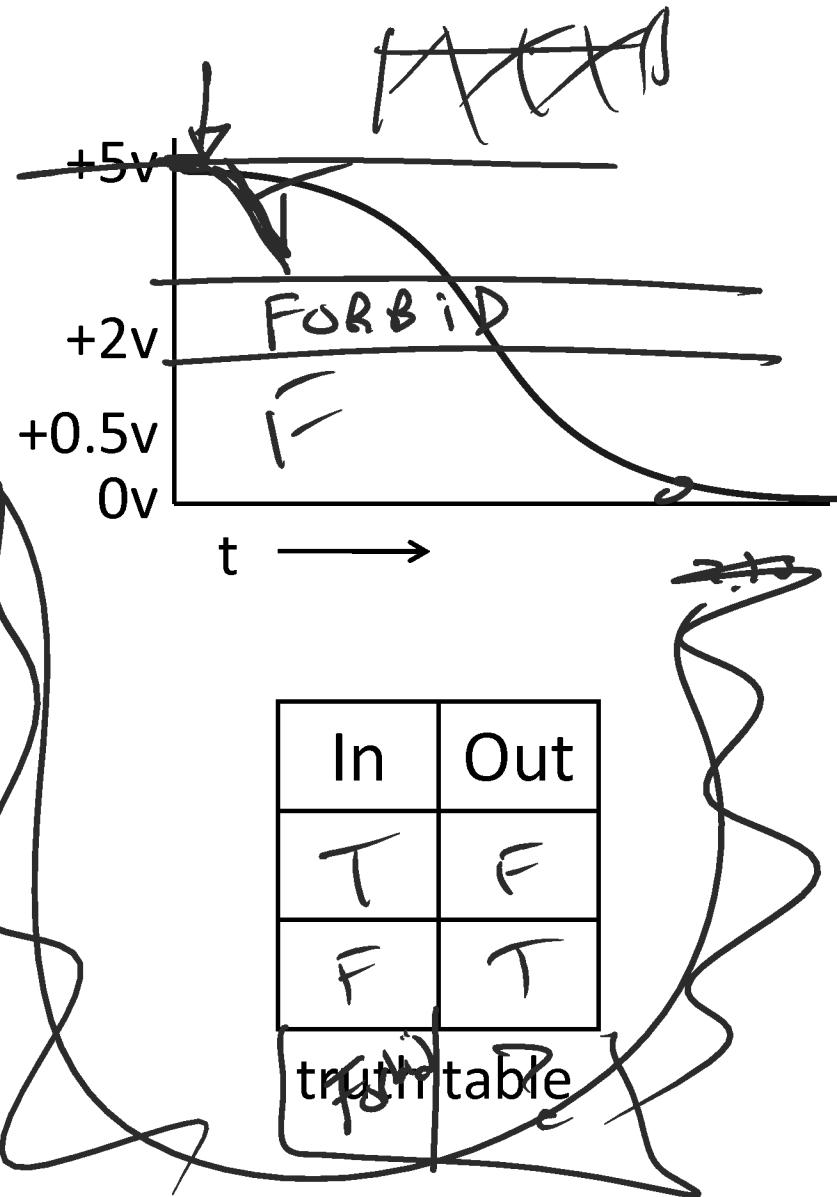
(complementary-symmetry metal–oxide–semiconductor)

- Power consumption = dynamic + leakage



In	Out
+5v	0v
0v	+5v

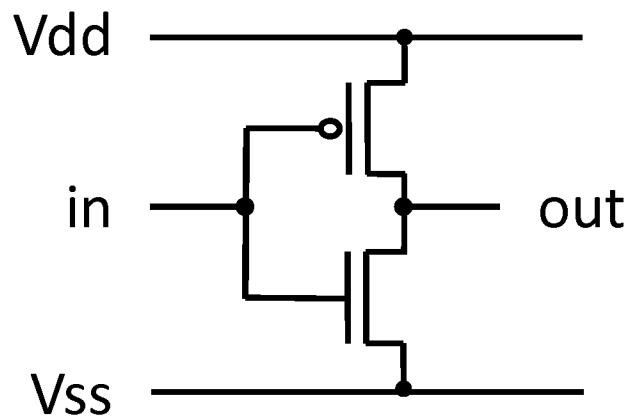
voltage



Conventions:

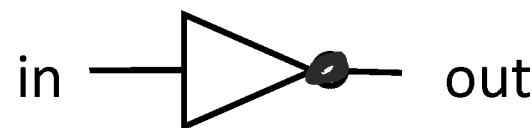
$V_{DD} = V_{CC} = +1.2V = +5V = hi = true = 1$

$V_{SS} = V_{EE} = 0V = gnd = false = 0$



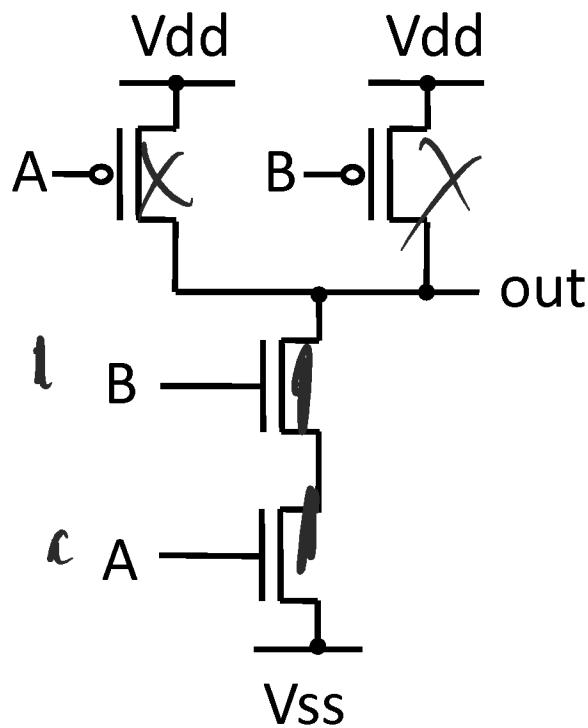
Function: NOT

- Symbol:



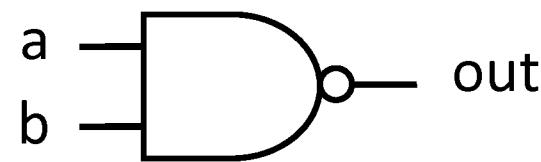
In	Out
0	1
1	0

Truth table

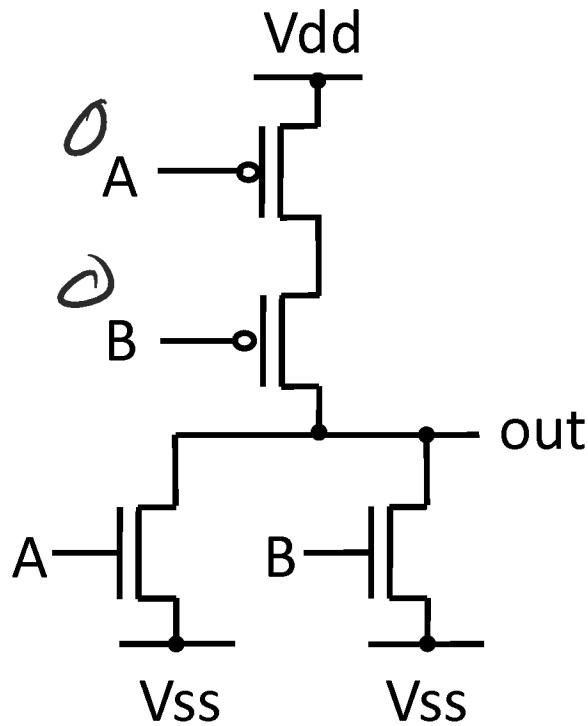


Function: NAND

- Symbol:

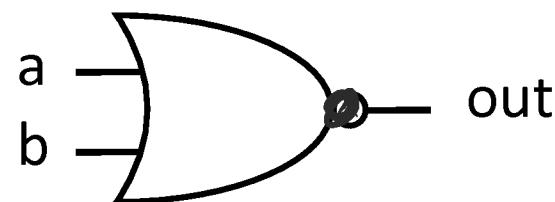


A	B	out
0	0	1
0	1	1
1	0	1
1	1	0



Function: NOR

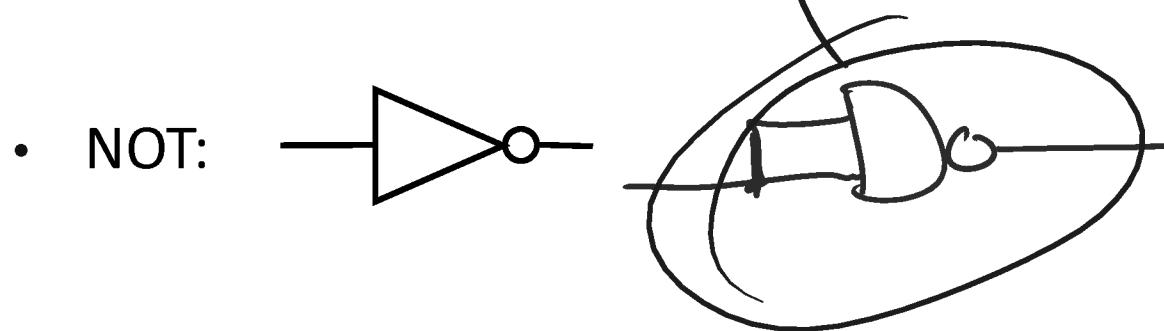
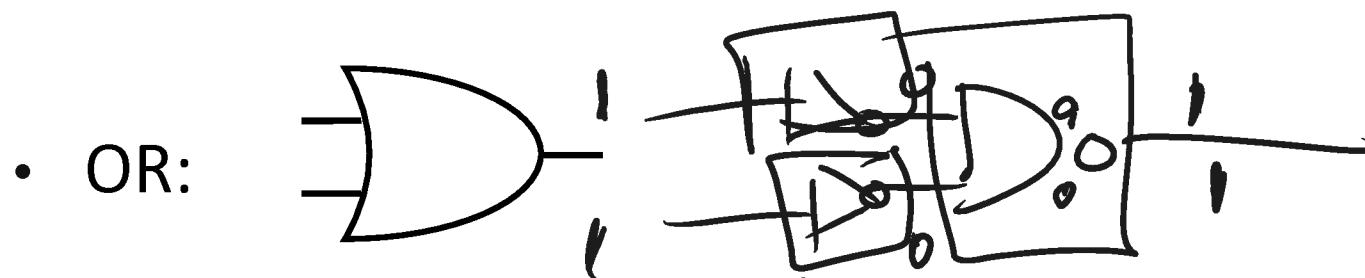
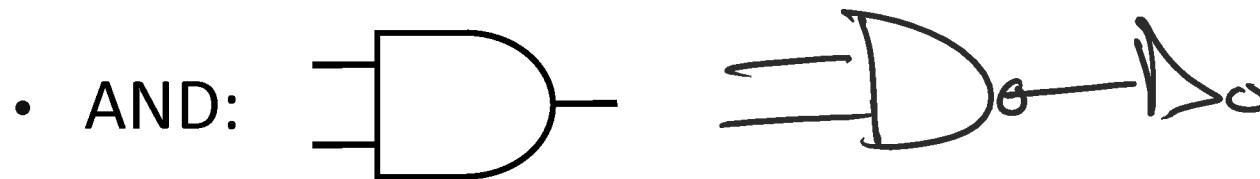
- Symbol:



A truth table for a NOR gate is shown, illustrating the function of the gate. The columns are labeled A, B, and out. The rows show all possible combinations of inputs A and B. The output 'out' is 1 when either A or B is 0, and it is 0 only when both A and B are 1. The row where both A and B are 1 is circled with a large oval.

A	B	out
0	0	1
0	1	0
1	0	0
1	1	0

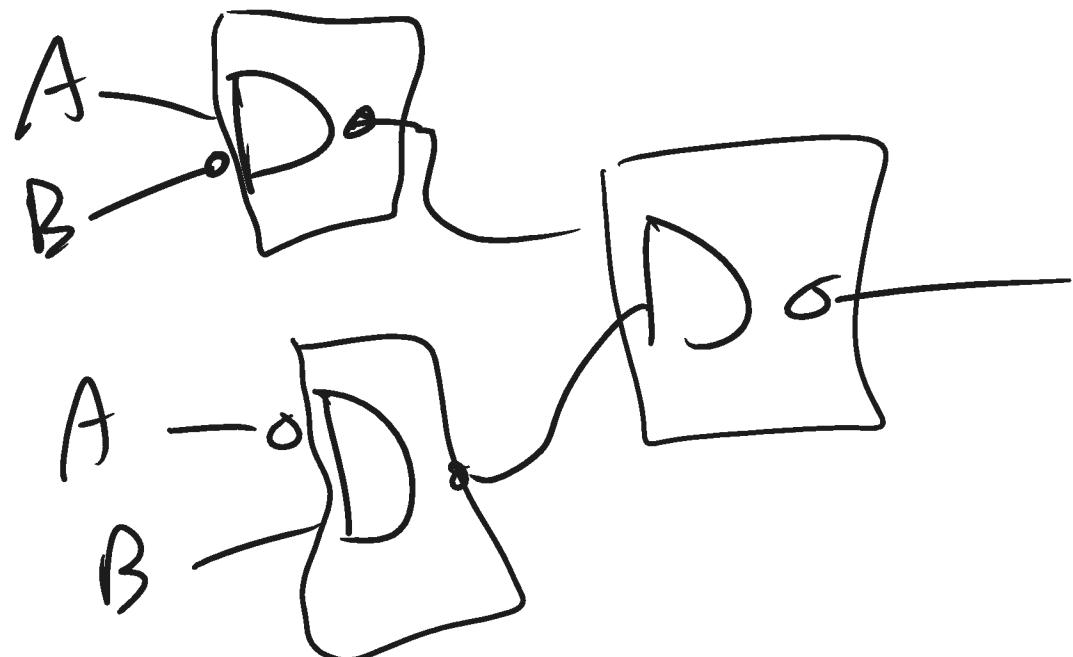
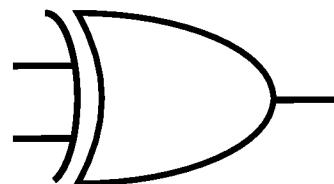
WST ( $\overline{A}$  and  $\overline{B}$ ) = ( $\overline{AND}(\overline{A}, \overline{B})$ ) or ( $\overline{WST}(\overline{A}) \overline{NOT}(\overline{B})$ )



# NAND is universal (so is NOR)

- Can implement any function with just NAND gates
  - De Morgan's laws are helpful (pushing bubbles)
- useful for manufacturing

E.g.: XOR ( $A, B$ ) = A or B but not both ("exclusive or")



Proof: ?

# Some notation:

- constants: true = 1, false = 0
- variables: a, b, out, ...
- operators:

$\begin{array}{ll} \text{AND}(a, b) & = a \cdot b \\ \text{OR}(a, b) & = a + b \\ \text{NOT}(a) & = \bar{a} \end{array}$	<p>The diagram shows three mappings from left-hand side expressions to right-hand side expressions. The first mapping is <math>\text{AND}(a, b) \rightarrow a \&amp; b</math>, where <math>a \&amp; b</math> is enclosed in a rounded rectangle. The second mapping is <math>\text{OR}(a, b) \rightarrow a   b</math>, where <math>a   b</math> is enclosed in a rounded rectangle. The third mapping is <math>\text{NOT}(a) \rightarrow !a</math>, where <math>!a</math> is enclosed in a rounded rectangle.</p> $\begin{array}{ll} \text{AND}(a, b) & \rightarrow a \& b \\ \text{OR}(a, b) & \rightarrow a   b \\ \text{NOT}(a) & \rightarrow !a \end{array}$
--	--

$$0 \cdot 0 = 0$$

$$0 \cdot 1 = 0$$

$$1 \cdot 0 = 0$$

$$1 \cdot 1 = 1$$

$$0 + 0 = 0$$

$$0 + 1 = 1$$

$$1 + 0 = 1$$

$$1 + 1 = 1$$

# Identities useful for manipulating logic equations

- For optimization & ease of implementation

$$a + 0 = a$$

$$a + 1 = 1$$

$$a + \bar{a} = 1$$

$$a \cdot 0 = 0$$

$$a \cdot 1 = a$$

$$a \cdot \bar{a} = 0$$

$$\overline{(a + b)} = \bar{a} \cdot \bar{b}$$

$$\overline{(a \cdot b)} = \bar{a} + \bar{b}$$

$$a + a \cdot b = a$$

$$a(b+c) = ab + ac$$

$$\overline{a(b+c)} = \bar{a} + \bar{b}\bar{c}$$

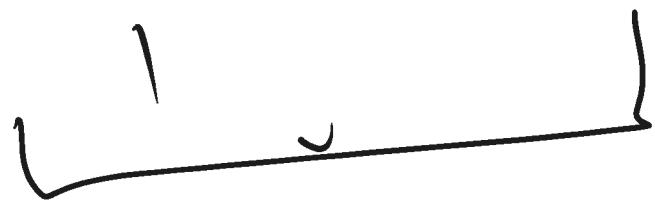
- functions: gates  $\leftrightarrow$  truth tables  $\leftrightarrow$  equations
- Example:  $(a+b)(a+c) = a + bc$

a	b	c	a+b	a+c	LHS	bc	RHS
0	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0
0	1	0	1	0	0	0	0
0	1	1	1	1	1	1	1
1	0	0	1	1	1	0	1
1	0	1	1	1	1	0	1
1	1	0	1	1	1	0	1
1	1	1	1	1	1	1	1

$$(a+b)(a+c)$$

$$\frac{a \cdot a + a \cdot c + b \cdot a}{a \cdot 1} + b \cdot c$$

$$a \underbrace{(1 + c + b)}_{1 + b} + b \cdot c$$



$$\underbrace{a \cdot 1}_{a} + b c + b c$$