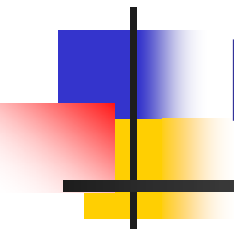
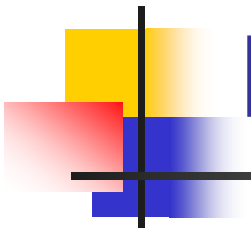


ECE/CS 314 Spring 2004

Section 9

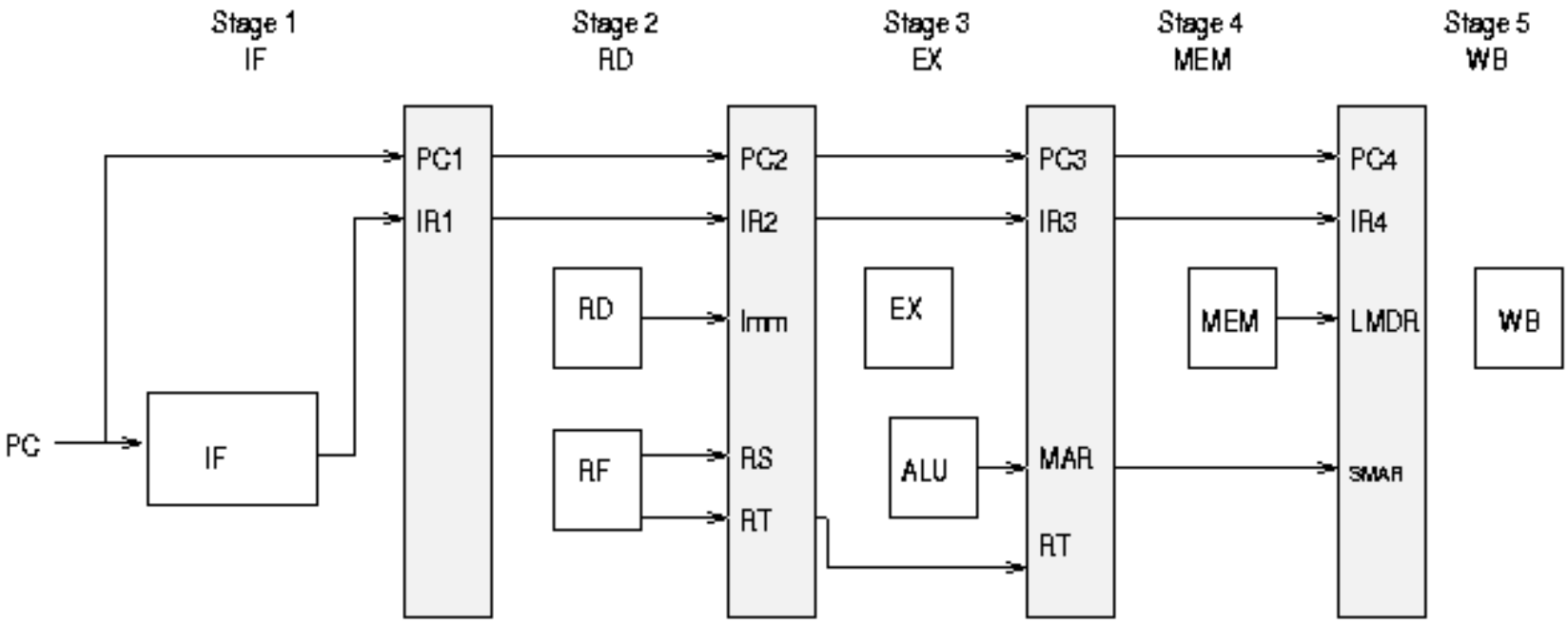
Project 4: Datapath Design



Part 1: Datapath Diagram

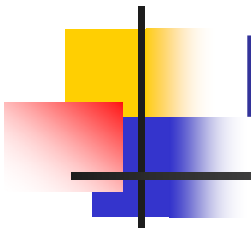
- Draw the 5-stage MIPS datapath in Visio
- Use the provided Visio template and stencil
- Be sure to include bypass paths
- PC-update must be shown in detail
- Logic to manipulate data word from memory does not have to be included (Draw a box and label it “Load parsing logic block”)

Part 1: Datapath Diagram



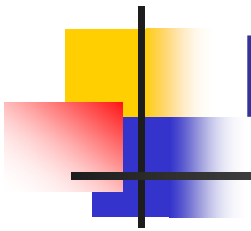
Visio Demo

- Most computers in PH318 have Visio installed
- MSDNAA accounts are being requested (free software!!!)



Part 2: Design Document

- Stage Description
  - Write a paragraph about what happens in each stage



Part 2: Design Document

- Signal List
  - Come up with a list of control signals for each stage
  - e.g. Mux selection signal in the WB stage
  - Some signals might be produced in one stage, but used in another

Part 2: Design Document

- Sample Execution

```
0x100:          sll    $0,$0,0          # nop
0x104:          sll    $0,$0,0
0x108:          sll    $0,$0,0
0x10c:          sll    $0,$0,0
0x110:          lw     $1,100($4)       # assume value = 17
0x114:          lui    $2,15
0x118:          add    $1,$1,$2
0x11c:          bgezal $1,skip
0x120:          sub    $3,$1,$1
0x124:          lui    $3,101
0x128:    skip: sw     $3,0($4)
0x12c:          sll    $0,$0,0          # nop
0x130:          sll    $0,$0,0
0x134:          sll    $0,$0,0
0x138:          sll    $0,$0,0
```

Part 2: Design Document

- Example

Cycle # \Signal	Instr. in WB	RA	RB	RW	WE
1	sll $0, $0, $0	0	0	0	0
2	sll $0, $0, $0	4	0 (or anything)	0	0
3	sll $0, $0, $0	0 (or anything)	0 (or anything)	0	0
4	sll $0, $0, $0	1	2	0	0
5	lw $1, 100($4)			1	1
6	lui $2, 15			2	1
7	add $1, $1, $2			1	1