



ECE/CS 314 Spring 2004

Section 10 Cache



Cache Example

- From spring 2003 prelim #2



Cache Example

- Given a cache with the following configuration:
 - Size 8 KB
 - Block size 64 bytes
 - Associativity 4-way
 - Valid bit yes
 - Replacement LRU
 - Write policy Write back



Cache Example

- How is the address broken down into tag, index, and offset?



Cache Example

- How is the address broken down into tag, index, and offset?

Tag	Index	Offset



Cache Example

- How is the address broken down into tag, index, and offset?

Tag	Index	Offset
21	5	6



Cache Example

- How much overhead (i.e. non-data storage) in each way?



Cache Example

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 - Overhead for each block:
 - Valid bit (1 bit)
 - Dirty bit (1 bit) = 23 bits/block
 - Tag bits (21 bits)



Cache Example

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 - Overhead for each block:
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 - Dirty bit (1 bit) = 23 bits/block
 - Tag bits (21 bits)
 - Number of blocks per way:
 - $8192(\text{bytes})/64(\text{bytes/block})/4(\text{ways}) = 32$ blocks



Cache Example

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 - Overhead for each block:
 - Valid bit (1 bit)
 - Dirty bit (1 bit) = 23 bits/block
 - Tag bits (21 bits)
 - Number of blocks per way:
 - $8192(\text{bytes})/64(\text{bytes/block})/4(\text{ways}) = 32$ blocks
 - Overhead per way:
 - $23 \text{ bits/block} * 32 \text{ blocks} = 736 \text{ bits} = 92 \text{ bytes}$



Cache Example

- Assume the same cache parameters. Determine whether the following accesses are misses or not; and if so, what type.



Cache Example

\$1=0x10000000 \$2=0x20000000
\$3=0x30000000 \$4=0x40000000

Access	Miss (Yes/No)	Type
lw \$20, 0(\$0)		
lw \$20, 4(\$1)		
lw \$20, 64(\$0)		
lw \$20, 16(\$0)		
lw \$20, 0(\$2)		
lw \$20, 0(\$3)		
lw \$20, 0(\$4)		
lw \$20, 0(\$1)		
lw \$20, 8(\$2)		



Cache Example

- A few lines of interest (showing top 20 bits of tag):

Index	Way 0	Way 1	Way 2	Way 3
0				
1				



Cache Example

- A few lines of interest (showing top 20 bits of tag):

Index	Way 0	Way 1	Way 2	Way 3
0	0x00000			
1				



Cache Example

\$1=0x10000000 \$2=0x20000000
 \$3=0x30000000 \$4=0x40000000

Access	Miss (Yes/No)	Type
lw \$20, 0(\$0)	Yes	Compulsory
lw \$20, 4(\$1)		
lw \$20, 64(\$0)		
lw \$20, 16(\$0)		
lw \$20, 0(\$2)		
lw \$20, 0(\$3)		
lw \$20, 0(\$4)		
lw \$20, 0(\$1)		
lw \$20, 8(\$2)		



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0	0x00000			
1				



Cache Example

- A few lines of interest (showing top 20 bits of tag):

Index	Way 0	Way 1	Way 2	Way 3
0	0x00000	0x10000		
1				



Cache Example

\$1=0x10000000

\$2=0x20000000

\$3=0x30000000

\$4=0x40000000

Access	Miss (Yes/No)	Type
lw \$20, 0(\$0)	Yes	Compulsory
lw \$20, 4(\$1)	Yes	Compulsory
lw \$20, 64(\$0)		
lw \$20, 16(\$0)		
lw \$20, 0(\$2)		
lw \$20, 0(\$3)		
lw \$20, 0(\$4)		
lw \$20, 0(\$1)		
lw \$20, 8(\$2)		



Cache Example

- A few lines of interest (showing top 20 bits of tag):

Index	Way 0	Way 1	Way 2	Way 3
0	0x00000	0x10000		
1				



Cache Example

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Index	Way 0	Way 1	Way 2	Way 3
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lw \$20, 0(\$2)	Yes	Compulsory
lw \$20, 0(\$3)	Yes	Compulsory
lw \$20, 0(\$4)		
lw \$20, 0(\$1)		
lw \$20, 8(\$2)		



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lw \$20, 16(\$0)	No	
lw \$20, 0(\$2)	Yes	Compulsory
lw \$20, 0(\$3)	Yes	Compulsory
lw \$20, 0(\$4)	Yes	Compulsory
lw \$20, 0(\$1)	Yes	Conflict
lw \$20, 8(\$2)		



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0	0x10000	0x40000	0x20000	0x30000
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lw \$20, 0(\$2)	Yes	Compulsory
lw \$20, 0(\$3)	Yes	Compulsory
lw \$20, 0(\$4)	Yes	Compulsory
lw \$20, 0(\$1)	Yes	Conflict
lw \$20, 8(\$2)	No	