Problem 9. VM address translation. (9 points):

The following problem concerns the way virtual addresses are translated into physical addresses.

- The memory is byte addressable.
- Memory accesses are to **1-byte words** (not 4-byte words).
- Virtual addresses have the following fields: VPN: [15-9], VPO: [8-0], TLBT: [15-10], TLBI: [9]
- Physical addresses have following fields: PPN: [12-9], PPO: [8-0], CT: [12-5], CI: [4-2], CO: [1-0]
- The TLB is 8-way set associative with 16 total entries, as shown.
- The cache is 2-way set associative, with a 4 byte line size and 16 total lines.

In the following tables, **all numbers are given in hexadecimal**. The contents of the TLB, the page table for the first 32 pages, and the cache are as follows:

TLB			
Index	Tag	PPN	Valid
0	09	4	1
	12	2	1
	10	0	1
	08	5	1
	05	7	1
	13	1	0
	10	3	0
	18	3	0
1	04	1	0
	0C	1	0
	12	0	0
	08	1	0
	06	7	0
	03	1	0
	07	5	0
	02	2	0

Page Table					
VPN	PPN	Valid	VPN	PPN	Valid
00	6	1	10	0	1
01	5	0	11	5	0
02	3	1	12	2	1
03	4	1	13	4	0
04	2	0	14	6	0
05	7	1	15	2	0
06	1	0	16	4	0
07	3	0	17	6	0
08	5	1	18	1	1
09	4	0	19	2	0
0A	3	0	1A	5	0
0B	2	0	1B	7	0
0C	5	0	1C	6	0
0D	6	0	1D	2	0
0E	1	1	1E	3	0
0F	0	0	1F	1	0

2-way Set Associative Cache												
Index	Tag	Valid	Byte 0	Byte 1	Byte 2	Byte 3	Tag	Valid	Byte 0	Byte 1	Byte 2	Byte 3
0	19	1	99	11	23	11	00	0	99	11	23	11
1	15	0	4F	22	EC	11	2F	1	55	59	0B	41
2	1B	1	00	02	04	08	0B	1	01	03	05	07
3	06	0	84	06	B2	9C	12	0	84	06	B2	9C
4	07	0	43	6D	8F	09	05	0	43	6D	8F	09
5	0D	1	36	32	00	78	1E	1	A1	B2	C4	DE
6	11	0	A2	37	68	31	00	1	BB	77	33	00
7	16	1	11	C2	11	33	1E	1	00	C0	0F	00

For the given virtual address, indicate the TLB entry accessed, the physical address, and the cache byte value returned **in hex**. Indicate whether the TLB misses, whether a page fault occurs, and whether a cache miss occurs.

If there is a cache miss, enter “-” for “Cache Byte returned”. If there is a page fault, enter “-” for “PPN” and leave parts C and D blank.

Virtual address: `1DDE`

A. Virtual address format (one bit per box)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

B. Address translation

Parameter	Value
VPN	0x
TLB Index	0x
TLB Tag	0x
TLB Hit? (Y/N)	
Page Fault? (Y/N)	
PPN	0x

C. Physical address format (one bit per box)

12	11	10	9	8	7	6	5	4	3	2	1	0

D. Physical memory reference

Parameter	Value
Cache offset	0x
Cache Index	0x
Cache Tag	0x
Cache Hit? (Y/N)	
Cache Byte returned	0x

E. How many entries does the page table have?
How many entries would it have if it were an inverted page table?

Problem 9. VM address translation. (9 points):

The following problem concerns the way virtual addresses are translated into physical addresses.

- The memory is byte addressable.
- Memory accesses are to **1-byte words** (not 4-byte words).
- Virtual addresses have the following fields: VPN: [15-9], VPO: [8-0], TLBT: [15-10], TLBI: [9]
- Physical addresses have following fields: PPN: [12-9], PPO: [8-0], CT: [12-5], CI: [4-2], CO: [1-0]
- The TLB is 8-way set associative with 16 total entries, as shown.
- The cache is 2-way set associative, with a 4 byte line size and 16 total lines.

In the following tables, **all numbers are given in hexadecimal**. The contents of the TLB, the page table for the first 32 pages, and the cache are as follows:

TLB			
Index	Tag	PPN	Valid
0	09	4	1
	12	2	1
	10	0	1
	08	5	1
	05	7	1
	13	1	0
	10	3	0
	18	3	0
1	04	1	0
	0C	1	0
	12	0	0
	08	1	0
	06	7	0
	03	1	0
	07	5	0
	02	2	0

Page Table					
VPN	PPN	Valid	VPN	PPN	Valid
00	6	1	10	0	1
01	5	0	11	5	0
02	3	1	12	2	1
03	4	1	13	4	0
04	2	0	14	6	0
05	7	1	15	2	0
06	1	0	16	4	0
07	3	0	17	6	0
08	5	1	18	1	1
09	4	0	19	2	0
0A	3	0	1A	5	0
0B	2	0	1B	7	0
0C	5	0	1C	6	0
0D	6	0	1D	2	0
0E	1	1	1E	3	0
0F	0	0	1F	1	0

2-way Set Associative Cache												
Index	Tag	Valid	Byte 0	Byte 1	Byte 2	Byte 3	Tag	Valid	Byte 0	Byte 1	Byte 2	Byte 3
0	19	1	99	11	23	11	00	0	99	11	23	11
1	15	0	4F	22	EC	11	2F	1	55	59	0B	41
2	1B	1	00	02	04	08	0B	1	01	03	05	07
3	06	0	84	06	B2	9C	12	0	84	06	B2	9C
4	07	0	43	6D	8F	09	05	0	43	6D	8F	09
5	0D	1	36	32	00	78	1E	1	A1	B2	C4	DE
6	11	0	A2	37	68	31	00	1	BB	77	33	00
7	16	1	11	C2	11	33	1E	1	00	C0	0F	00

For the given virtual address, indicate the TLB entry accessed, the physical address, and the cache byte value returned **in hex**. Indicate whether the TLB misses, whether a page fault occurs, and whether a cache miss occurs.

If there is a cache miss, enter "-" for "Cache Byte returned". If there is a page fault, enter "-" for "PPN" and leave parts C and D blank.

Virtual address: `1DDE`

A. Virtual address format (one bit per box)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Answer: 0001 1101 1101 1110

B. Address translation

Parameter	Value
VPN	0x0E
TLB Index	0x0
TLB Tag	0x07
TLB Hit?	N
Page Fault?	N
PPN	0x1

C. Physical address format (one bit per box)

12	11	10	9	8	7	6	5	4	3	2	1	0

Answer: 0 0011 1101 1110

D. Physical memory reference

Parameter	Value
Cache offset	0x2
Cache Index	0x7
Cache Tag	0x1E
Cache Hit?	Y
Cache Byte returned	0xF

E. How many entries does the page table have? 2^7 = 128
How many entries would it have if it were an inverted page table? 2^4 = 16

[20pts] 4. Oldie but Goodie

The **PDP11** was a series of computers sold by Digital Equipment Corp. (DEC) from 1970 and into the nineties. A PDP11 computer has a 16-bit virtual address space, where each address identifies a byte, for a total of 64 Kbytes. A page is 2^{13} bytes = 8 Kbytes, and thus the virtual address space of a process consisted of 8 pages. A page table entry (PTE) had a 9-bit frame (= physical page) number, a Valid bit, and a Writable bit.

a) [5pts] What is the maximum physical memory (in Kbytes) in a PDP11?
(A Kbyte is 1024 bytes.)

b) [9pts] Consider the following page table of a process:

Page	Valid	Frame	Writable
0	yes	0x003	no
1	yes	0x001	no
2	yes	0x008	yes
3	no	N/A	N/A

Page	Valid	Frame	Writable
4	no	N/A	N/A
5	no	N/A	N/A
6	no	N/A	N/A
7	yes	0x004	yes

Fill in the following table:

Virtual Address	Valid (yes, no)	Physical Address (if valid) in hexadecimals	Writable (yes, no)
0x1234			
0x4321			
0x8888			

c) [6pts] The Bogux O/S running on the PDP11 uses "Local Replacement", meaning that it assigns a certain number of physical frames to each process. As a result, two processes never contend for the same frame. However, if a lot of processes are running, the number of frames per process may well be fewer than 8. Assume a situation in which each process has three frames. Suppose the page reference string of some process is

0, 7, 2, 0, 7, 1, 0, 3, 1, 2

Initially no pages are mapped to physical frames. Now consider the state of the process's page table after the first 7 references (i.e., after page accesses 0 7 2 0 7 1 0). Which (up to three) pages are mapped at this time assuming one of the following page replacement schemes, and how many page faults have occurred then. Also show in the last column how many page faults occur in total after all 10 references?

Scheme	all page numbers of mapped pages **after 7 references** (3 max.)	#page faults **after 7 references**	#page faults total (**after 10 references**)
First In First Out (by way of example)	0 1 2	5	7
LRU (Least Recently Used)			
OPT (Belady)			

[20pts] 4. Oldie but Goodie

The **PDP11** was a series of computers sold by Digital Equipment Corp. (DEC) from 1970 and into the nineties. A PDP11 computer has a 16-bit virtual address space, where each address identifies a byte, for a total of 64 Kbytes. A page is 2^{13} bytes = 8 Kbytes, and thus the virtual address space of a process consisted of 8 pages. A page table entry (PTE) had a 9-bit frame (= physical page) number, a Valid bit, and a Writable bit.

a) [5pts] What is the maximum physical memory (in Kbytes) in a PDP11?
(A Kbyte is 1024 bytes.)

2^{13+9} = 4,096 Kbytes

b) [9pts] Consider the following page table of a process:

Page	Valid	Frame	Writable
0	yes	0x003	no
1	yes	0x001	no
2	yes	0x008	yes
3	no	N/A	N/A

Page	Valid	Frame	Writable
4	no	N/A	N/A
5	no	N/A	N/A
6	no	N/A	N/A
7	yes	0x004	yes

Fill in the following table:

Virtual Address	Valid (yes, no)	Physical Address (if valid) in hexadecimals	Writable (yes, no)
0x1234	yes	0x07234	no
0x4321	yes	0x10321	yes
0x8888	no	N/A	no

c) [6pts] The Bogux O/S running on the PDP11 uses "Local Replacement", meaning that it assigns a certain number of physical frames to each process. As a result, two processes never contend for the same frame. However, if a lot of processes are running, the number of frames per process may well be fewer than 8. Assume a situation in which each process has three frames. Suppose the page reference string of some process is

0, 7, 2, 0, 7, 1, 0, 3, 1, 2

Initially no pages are mapped to physical frames. Now consider the state of the process's page table after the first 7 references (i.e., after page accesses 0 7 2 0 7 1 0). Which (up to three) pages are mapped at this time assuming one of the following page replacement schemes, and how many page faults have occurred then. Also show in the last column how many page faults occur in total after all 10 references?

Scheme	all page numbers of mapped pages **after 7 references** (3 max.)	#page faults **after 7 references**	#page faults total (**after 10 references**)
First In First Out (by way of example)	0 1 2	5	7
LRU (Least Recently Used)	0 1 7	4	6
OPT (Belady)	0 1 2	4	5